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(54) Data recording/reproducing apparatus using a recording disk.

(57) An equalizer apparatus is to be applied to a disk recording medium of DBF, for which there is used a sampling clock reproduced from the clock pit recorded on a disk recording medium. A fixed equalizer block comprising an analog to digital converter, a memory and a two-dimension equalizer suppresses the wave interference from the adjacent tracks and can reduce the error rate of the reproduced data by cross-talk even in case of narrowing of the track pitch. Further, by adding to the equalizer a sign detector, an FIR low-pass filter and a coefficient control circuit to make it a blind equalizer block, the interference fluctuation attributed to linear recording density, recording power irregularity, light spot, tracking error, etc. can be automatically compensated to suppress such fluctuation. Further, By the construction of the blind equalizer block, the errors of clock timing and its fluctuation can be automatically compensated with good efficiency.

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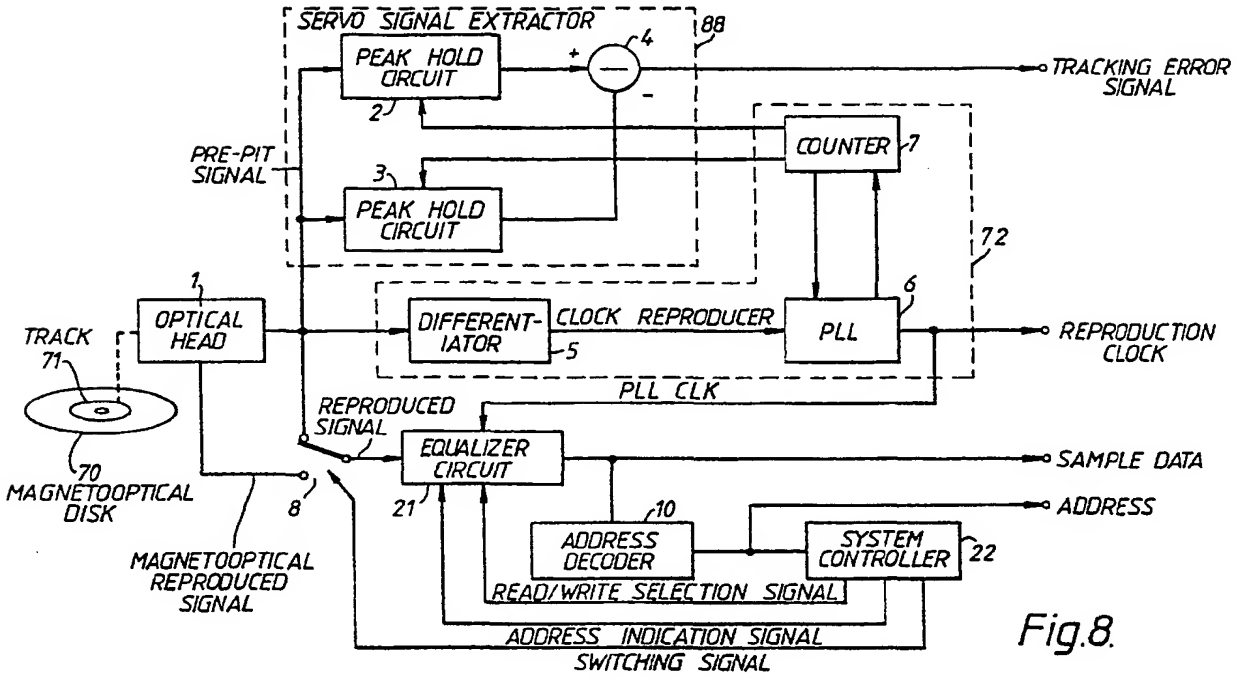

Fig.8.

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DATA RECORDING/REPRODUCING APPARATUS USING A RECORDING DISK

In recent years, vigorous developments of optical disk apparatuses have been in effect as the recording apparatuses having large capacities. The data format used for recording and reproducing data in an optical disk apparatus is mainly classified into two types of continuous composite servo format and Discrete Block servo Format (hereinafter to be abbreviated as DBF) from the detection method of the tracking signal of light spot and the groove shape on the disk medium. Of these, the present invention relates to an equalizer of the optical disk apparatus using DBF and an optical disk recording/reproducing apparatus.

Hitherto, DBF has its characteristics in easiness of detection of tracking signal and stability of clock detection of the recorded and reproduced data, and is designed to detect all the timings using the clock pits written on the disk.

Hereinafter, referring to the drawing, explanation will be given on the signal reproducing section of the conventional optical disk recording/reproducing apparatus as mentioned above.

Fig. 1 shows the signal reproducing section of the conventional magnetooptical disk; Fig. 2 and Fig. 3 are the waveform diagrams for illustrating the operation thereof; and Fig. 4 is a circuit diagram for the equalization cricuit of the signal reproducing section of the conventional magnetooptical disk.

In Fig. 1, the part 1 shows an optical head. The optical head is composed of a laser, a lens, an actuator, a polarized beam splitter, a pin photodiode, a prepit signal reproducing circuit, a magnetooptical signal reproducing circuit, etc. The part 70 is an optcal disk, 71 is a track, 2 and 3 are the peak hold circuits, 4 is a subtractor, 5 is a differentiator, 7 is a counter, 8 is a switch, 9 is an equalization circuit, 10 is an address decoder, 11 is a system controller. 72 is a clock reproducer. The clock reproducer 72 is composed of a differentiator 5, a phase locked loop circuit 6, and a counter 7. 88 is a servo signal extractor. The servo signal extractor 88 is composed of a peak hold circuits 2, 3 and a subtractor 4. In Fig. 4, the part 12 is an analog to digital converter. 13 ~ 15 are D flip-flops (hereinafter to be abbreviated as D-FFS), 16 ~ 18 are multipliers, and 19 and 20 are adders.

In Fig. 1, the optical head 1 outputs a focus error signal by an optical spot formed on the magnetooptical disk 70 and outputs the addresses, wobble marks and clock-pits which are unevenly recorded as shown in Fig. 2 as the pre-recording signals of the change in the reflected light amount.

The data format for recording and reproducing the 3.5 inch magnetooptical disk with enlargement of the track 71 of the disk 70 in Fig. 1 is shown in Fig. 2. As shown in Fig. 2 (a) ~ (c) , the data format for recording and reproducing in the 3.5 inch magnetooptical disk is formed by dividing 1 track of a one circulation into 22 sectors, with 1 sector comprising 76 blocks. Of 76 blocks, the 0th block ~ second block are the header blocks, being the addresses showing the sector mark, sector number, and track number. The third block ~ 75th block are the data blocks, in which 1 block is composed of the two servo- bytes and eight data bytes. These servo-bytes are composed of the wobble marks for tracking error detection and the clock-pits for clock reproduction, as shown in Fig. 2 (c). In Fig. 1, the differentiator 5 differentiates the clock-pit signal which is an input signal and outputs it. The phase locked loop circuit 6 has the free running frequency of 110 times the repeating frequency of the clock-pit signal; it accepts the output of said differentiator 5 only in the vicinity of the reproduction timing of the clock-pit by the indication signal of the counter 7; performs phase comparison of the reproduced clock output with the signal made by dividing the reproduced clock output into 110 sections with a counter 7 and synchronizes it. The counter 7 is a 110 divisional counter as aforementioned, which divides the aforementioned reproduced clock into 110 sections and at the same time outputs the timing indication signal of the said clock pit and the timing indication signal of the wobble marks. By the abovementioned operations, the clock reproducer 72 reproduces the clock.

The peak holds 2 and 3 output by holding the maximum values V1 and V2 of the wobble mark signals in the timings indicated by the counter 7 as in Fig. 2 (d), and the subtractor 4 outputs the difference between the peak holds 2 and 3 as a tracking error signal. The servo signal extractor 88 outputs the tracking error signal by the above operation. Here, the address signal and the magnetooptical signal are recorded and reproduced in 4-11 modulation. In the 4-11 modulation, the data in the length of 11 bits is allocated to one symbol of the length of 1 byte before modulation, and as its rule modulation is made so that the number of the code "1" after the modulation becomes four in the one symbol of 11 bits. Accordingly, to 8 bytes of the data section in one block, the data of 88 bits are recorded and reproduced. This state corresponds to 110 bits in the length of one block. The write-in clock to be used for recording the magnetooptical signal is a reproduced clock reproduced from the aforementioned clock-pit, and similarly, for equalization and identification of data, the aforementioned reproduced clock is used. The address signal and the data signal outputted from the optical head 1 are connected to the switch 8. The switch 8 changes

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over the address signal and the data signal using the switching signal of the system controller 11.

A circuit diagram of the equalization circuit 9 is shown in Fig. 4. The output of the switch 8 is inputted to the analog to digital (AD) converter 12. the AD converter 12 converts the analogue address signal and optical magnetic signal into digital signals. The sampling signal is a reproduced clock of the phase locked loop circuit 7. The clocks of D-FFS 13 - 15 are also similarly the aforementioned reproduced clocks, which output the outputs of AD converter 12 by sequentially delaying by one cycle of the above reproduced clock to the multipliers 16 - 18. The multipliers 16 - 18 multiply the aforementioned delayed signals by the coefficients of W(-1) - W(1) and output them to the adders 19 and 20. D-FF 13 - 15S, multiplirs 16 - 18, adders 19 and 20 constitute a transversal filter or 3 taps, and its transfer function H1 is expressed, as:

$$H1 = W(-1)\cdot X(n+1) + W(0)\cdot X(n) + W(1)\cdot X(n-1)$$

Its characteristic varies according to the coefficients of the multipliers 16 - 18. The equalization circuit 9 has an effect of suppressing the wave interference by the adjacent bits of the reproduced signals S6 - S8 as shown in Fig. 3 (a) . The address decoder 10 detects the address signal out of the equalization circuit 9 and demodulates the current address. The system controller 11 operates by taking in the output of the address demodulator 10 to output the changeover signal for changing over between the address signal and the data signal to the switch 8.

As one of the characteristics of the optical disk there is given a large memory capacity. This is because, due to the fact that the linear density is equivalent to that of the magnetic disk apparatus at more than 20 Kbpi and the inter-track pitch of the recording track is small at about 1.6 microns, large area density can be obtained. At present, with this characteristic developed further, a further demand for high density has arisen. As a method for realizing this requirement, it is general to expect an increase in the linear density and to reduce the wave interference by using the equalization circuit in the conventional data reproducing section. As another direction, it is considered to make the track pitch smaller to increase the area density. When the track pitch becomes not more than 1 micron, the cross talk from the adjacent track increases. However, in the equalization circuit in the signal reproduction section of the conventional magnetooptical disk, there has been given no consideration at all to the interference from the adjacent track, and there has been a defect of limitation to attaining high density.

An object of the present invention is to provide the two-dimensional fixed and blind equalizers designed to suppress the wave interference from the adjacent tracks which have never been considered in the conventional one-dimensional equalization circuit and a data recording/reproducing apparatus using a recording disk using such two-dimensional equalizer.

In order to attain the above object, a data recording/reproducing apparatus using a disk recording medium has an equalizer block comprising: an analog to digital converter for sampling, quantitizing and outputting reproduced signals from the disk recording medium; a memory for storing signal trains of a plurality of tracks outputted from said analog to digital converter; and a wave equalizer for reading out simultaneously the signal trains of a plurality of tracks stored in said memory and performing equalization with respect to both of a wave interference in the longitudinal direction of each track and a wave intereference from an adjacent track.

By the above construction, it is possible to suppress the wave interference from the adjacent track and minimize the reproduced data error rate by cross-talk even in case that the track pitch is narrow. Further, by making the equalizer into a blind equalizer, wave interference fluctuations attributed to linear recording density, irregularity of recording power, optical spot, tracking error, etc. are automatically corrected and suppressed. Furthermore, the blind equalizer may be so constructed as to correct automatically in good efficiency the error and fluctuation of the clock timing.

Fig. 1 is a signal reproducing section of the conventional magnetooptical disk;

Fig. 2 and Fig. 3 are the wave diagrams for illustrating the operation thereof;

Fig. 4 is a circuit diagram of the equalization circuit for the signal reproducing section of the conventional magnetooptical disk;

Fig. 5 is an illustrative view of the optical spot shape;

Fig. 6 is an illustrative view of the 2 dimension disposition of sampling of the reproduced signal;

Fig. 7 is an illustrative view of the factors for fluctuation of the wave interference;

Fig. 8 is a block diagram of the data reproducing section of the present invention embodiment;

Fig. 9 is a circuit diagram of the first embodiment of the fixed equalizer block according to the present invention;

Fig. 10 is a circuit diagram of the second embodiment of the fixed equalizer block according to the present invention;

Fig. 11 is a circuit diagram of the equalizer of the first embodiment of the blind equalizer block according to the present invention;

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Fig. 12 is a circuit diagram of the equalizer of the second embodiment of the blind equalizer block according to the present invention;

Fig. 13 is a circuit diagram of the coefficient control circuit of the first and the second embodiments of the blind equalizer block according to the present invention;

Fig. 14 is a circuit diagram of the equalizer of the third embodiment of the blind equalizer block according to the present invention; and

Fig. 15 (a) and (b) are the circuit diagrams of the coefficient control circuits of the third embodiment of the blind equalizer block according to the present invention.

Hereinafter, in these drawings, the parts having the same functions are indicated in the same numbers and explanations thereof omitted.

Explanation on the first embodiment of the fixed equalizer block according to the present invention is given using the block diagram of Fig. 8 and the circuit diagram of the equalizer of Fig. 9.

In Fig. 8, the part 1 is an optical head. 70 is a magnetooptical disk, 71 is a track, 2 and 3 are the peak hold circuits, 4 is a subtractor, 5 is a differentiator, 6 is a phase locked loop circuit, 7 is a counter, 8 is a switch, 21 is an equalizer block, 10 is an address decoder, 22 is a system controller, 72 is a clock reproducer, and the clock reproducer 72 is composed of a differentiator 5, a phase locked loop circuit 6 and a counter 7. The part 88 is a servo signal extractor, and the servo signal extractor 88 is composed of a peak hold circuits 2, 3 and a subtractor 4. These relations are the same as in the block diagrams of the following embodiments.

In Fig. 8, the clock reproducer 72 generates a reproduced clock from clock pits in the same manner as in the conventional embodiment.

Similarly, the servo signal extractor 88 also outputs a tracking error signal from the maximum values V1 and V2 of the wobble mark signals as shown in Fig. 2 (d). The address signal and the data signal outputted from the optical head 1 are connected to the switch 8. The switch 8 changes over the address signal and the data signal according to the changeover signal from the system controller 22. The equalizer block 21 performs the equalization using the output of the phase locked loop circuit 6, the read/write selection signal for RAM and the address indication signal for RAM of the system controller 22. The address decoder 10 detects the address signal out of the outputs of the equalizer block 21 and decodes the current address. The system controller 22 is operated by taking in the output of the address decoder 10 to output the selection signal for changing over between the address signal and the data signal to the switch 8, and output the read/write selection signal for RAM and the address indication signal for RAM to the equalizer block 21. Of the equalizer 21 of Fig. 8, the circuit diagram of the first embodiment of the fixed equalizer block is shown in Fig. 9.

In Fig. 9, the part 23 is an analog to digital converter, 24 and 25 are RAMs, 26 - 30, 40 - 44, 55 - 59 are D - FFS, 31 - 35, 45 - 49, 60 - 64 are multipliers, and 36 - 39, 50 - 54, 65 - 69 are adders. 89 is an equalizer. The equalizer 89 is composed of D-FFS 26 - 30, multipliers 31 - 35 and adders 36 - 39. 90 is an equalizer. The equalizer 90 is composd of D-FF 40 - 44, multipliers 45 - 49 and adders 50 - 53. 138 is similarly an equalizer, and is composed of D-FF 55 - 59, multipliers 60 - 64 and adders 65 - 68.

In Fig. 9, the analog to digital converter 23 effects analog to digital conversion of the address signal and the data signal of the analog signals which are the outputs of the switch 8 into the digital signals. The analog to digital converter 23 employs an output of the phase locked loop circuit 6 as a sampling clock. The frequency of the reproduced clock signal is the same as the channel bit rate of the recorded and reproduced data. The output of the analog to digital converter 23 is 8 bits. The output of the analog to digital converter 23 is memorized in RAMs 24 and 25. The capacity of each of the RAMs 24 and 25 is the capacity capable of recording the data of 1 track. RAMs 24 and 25 use the output of the phase locked loop circuit as clock and change over between the reading and the writing of the data by the read/write selection signal for RAM which is the output of the system controller 22. Also, the addresses of the RAMs 24 and 25 are changed over by the address indication signal for RAM of the system controller 22.

Now, it is assumed to perform the optimal equalization of the mth track. When the RAM 24 outputs the data of the mth track, the RAM 25 outputs the data with delay of 1 track from the output of the RAM 24, so that it outputs the data of the (m - 1)th track. Also, at that time the AD converter 23 outputs the data of the (m + 1)th track.

The equalizers 89, 90 and 138 are the 5-tap transversal filters, and the equalizer 89 performs equalization of the data of the (m - 1)th track. The equalizer 90 performs equalization of the mth track, and similarly, the equalizer 138 performs equalization of the (m + 1)th track. The adder 54 adds the outputs of the equalizer 89 and the equalizer 90, and the adder 69 adds the outputs of the aforementioned adder 54 and the equalizer 138.

Fig. 6 is an illustrative view of the 2 dimension arrangement of the sampling of the reproduced signal. In

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Fig. 6, the white circles represent the clockpits and the black circles signify the positions of the read-out clocks.

As shown in Fig. 6, when the 3 X 5-tap coefficient matrix for obtaining the equalization output from the sample value matrix for 5 units per 1 track and the adjacent 3 track portions x(m,n) (m = i - 1, i, i + 1, n = j - 1, j, j + 1) is assumed to be W (k,1) (k = -1, 0, 1, l = -2, -1, ... 2), the output of the equalizer of Fig. 9, y(m, n) is:

$$y(m,\ n) = \sum_{k=-1}^{1} \sum_{l=-2}^{2} W(k,\ 1) \cdot X(m - k,\ n - l) \qquad (1)$$

Fig. 5 is an illustrative view of the optical spot shape, in which the central ellipse shows the intensity distribution of the optical spots, and, of the circles on the track, the larger circles show the read clock positions and the smaller circles show the write clock positions. As shown in Fig. 5, the tap coefficient W(k, l) of the equalizer block is determined according to the optical spot shape, recorded pit shape, etc. In general, the optical spot in which the intensity distribution can be approximated by Gaussian distribution is dominant to its characteristic, so that the coefficient matrix W(k,l) becomes:

$|W(k,0)| > |W(k, \pm 1)| > |W(k, \pm 2)|\ k = -1,0,1\ |W(0,1)| > |W(\pm 1,l)|\ l = -2,-1,.....2$

where, | | shows the absolute value.

By selecting the coefficient matrix as above W(k, l) , the equalizer 89 and the equalizer 138 are operated to suppress the crosstalk between the adjacent tracks, and the equalizer 90 is operated to perform the optimum equalization of the data of the mth track.

By the abovementioned construction of the 2-dimensional equalizer block, there can be realized a fixed equalizer block and an optical disk recording/reproducing apparatus using such a fixed equalizer block in which both the wave interference from the adjacent tracks and the wave interference of the adjacent bits are suppressed to perform the optimum equalization, and even in case of narrowing of the track pitch, the error rate of the reproduced data by crosstalk can be reduced.

Next, explanation is given on the second embodiment of the fixed equalizer block in which the optical spot shape is symmetric with respect to the longitudinal direction and the latitudinal direction of the track.

Fig. 10 shows a circuit diagram of the second embodiment of the fixed equalizer block as the equalizer block 21.

In Fig. 10, the numerals 73 - 75 and 80 - 82 are D-FFs, 76 - 78 and 83 - 85 are multipliers, and 79, 86, and 87 are adders. 139 is an equalizer. The equalizer 139 is composed of D-FFs 73 - 75, multipliers 76 - 78 and adder 79. 140 is an equalizer. The equalizer 140 is composed of D-FFs 80 - 82, multipliers 83 - 85 and adders 86 and 87. The equalizers 139 and 140 are each composed of a 3 tap transversal filter.

When the intensity distribution of the light spot is symmetrical with respect to the longitudinal direction and the latitudinal direction, the coefficient matrix w(K, l) becomes:

$W(k, l) = W1(k) \cdot W2(l) \qquad (2),$

so that the 2-dimensional coefficient W(k, l) is separable into the coefficient in the longitudinal direction in W1(k) and the coefficient in the latitudinal direction W2(l) Accordingly, the equalizer is separable into the longitudinal direction and the latitudinal direction of the track, and the output y(m, n) of the equalizer block 21 becomes:

$$y(m,\ n) = \sum_{k=-1}^{1} W1(k) \cdot \sum_{l=-1}^{1} W2(l) \cdot X(m - k,\ n - l) \qquad (3)$$

where, $k = -1,\ 0,\ +1,\ l = -1,\ 0,\ +1$

The equalizer 139 is operated to eliminate the cross talk from The adjacent track, and the equalizer 140 to eliminate the wave interference from the adjacent bits in the longitudinal direction of the track.

By the abovementioned construction, there can be realized a fixed equalizer of simple construction and

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an optical disk recording/reproducing apparatus using such a fixed equalizer in which, when the intensity distribution of the light spot is symmetrical with respect to the longitudinal direction and the latitudinal direction of the track, the wave interference from the adjacent tracks and the wave interference from the adjacent bits are suppressed to perform the optimum equalization, and even in case of narrowing of the track pitch, the error rate of the reproduced data by crosstalk can be reduced.

The abovementioned embodiment is to give the coefficient to the multiplier in a fixed state. However, by adaptively varying it, the equalization characteristic having the higher effect can be given.

Fig. 5 shows an illustrative view on the light spot shape. For example, in the swing arm supporting type optical system, the axis of the elliptical light spot intensity distribution as shown in Fig. 5 frequently varies according to the position on the disk for recording and reproducing, i.e., address, and in other system as well, the linear recording density varies according to the address. Therefore, there arises a necessity for the coefficient of the equalizer to be frequently varied. The causes for variation of the 2-dimensional recording and reproducing characteristics may be summarized as shown in Fig. 7.

As shown in Fig. 7, the factors for determining the equalization characteristic are mainly classified into the light spot shape related to the condition in recording, recording power, recording clock timing, focus, shape of recording pit and position thereof formed by fluctuation of tracking, light spot shape related to the condition in reproducing, tracking, focus, and adjacent symbols and intersymbol interference in the track direction by variation of sampling clock timing. Accordingly, by giving adequate desired signal, adapting of the coefficient to suppress the interference by adaptively following these variations becomes possible. As this adaptive algorism, there can be applied Least Mean Square error method (LMS method) (e.g., literature: B. Widrow, S. D. Stearns, "Adaptive Signal Processing, "Prentice-Hall, 1985), and the like extensively used in general. As the desired signal which becomes necessary here, the equalized output is sign detected, and, based on the result thereof, determination may be made in consideration of the non-distortion condition of intersymbol interference according to the modulation system in use.

Hereinafter, the first embodiment of the blind equalizer block is described.

Fig. 11 is a circuit diagram of an equalizer of the first embodiment of the blind equalizer block, and Fig. 13 is a circuit diagram of the coefficient control circuit of the first embodiment of the blind equalizer block.

In Fig. 11, 91 - 95, 105 - 109 and 120 - 124 are D-FFs, 96 - 100, 110 - 114 and 125 - 129 are multipliers, 101 - 104, 115 - 119 and 130 - 134 are adders, 136 is a comparator, and 135 - 137 are subtractors. 270 is a sign detector. The sign detector 270 is composed of a subtractor 135 and a comparator 136.

In Fig. 13, 195 - 239 are multipliers, 240 - 254 are D-FFs, and 255 - 269 are adders.

In Fig. 11, the basic equalizer unit composed of D-FFs 91 - 95, 105 - 109 and 120 - 124, multipliers 96 -100, 110 - 114 and 125 - 129, and adders 101 - 104, 115 -119 and 130 - 134 is identical with that shown in Fig. 9. The sign detector 270 gives the subtractor 135 a threshold level Th, and detects the sign of the original modulation signal from the size relation between y(m, n) and Th, and outputs a(m, n) [a(m, n) = 0, 1]. In this case, when the adaptation of the equalization characteristic is insufficient, there is a possibility for the identification error to become large, thus having effect upon the convergence charcteristic of adaptive algorism. But it is known that ultimately the equalization characteristic converges to a vicinity of the optimum characteristic. The desired signal to the sign detector output a(m, n) is assumed to be d(m, n). The non-distortion condition of the intersymbol interference of the present invention is assumed to satisfy Nyquist's the first basis in respect of either the longitudinal direction or the latitudinal direction of the track. (cf. Literature; W. R. Boennet, J. R. Davey, "Data Transmission" McGraw-Hill, 1965).
In this case, the relation becomes:

$$d(m, n) = a(m, n) \quad (4)$$

Accordingly, as the desired signal d(m, n) , the error signal e(m, n) may be operated using the sign detector output a(m, n). In other words, the substractor 137 outputs the difference between the equalizer output y(m, n) and the desired signal a(m, n) as an error signal e(m, n).

$$e(m, n) = d(m, n) - y(m, n) = a(m, n) - y(m, n) \quad (5)$$

The coefficient control circuit of Fig. 13 is a circuit to change over the 3 X 5 coefficient matrix W(k, 1) of the equalization circuit of Fig. 11.

The coefficient control circuit of Fig. 13 is to realize the adaptive algorism of the LMS method, in which, in order to minimize the minimum error average of the error signal e(m, n) of the equalizer of Fig. 11, the coefficient matrix is renewed according to the following equation. (cf. Literature: M. M. Hadhoud, D. W. Thomas, "The Two-Dimensional Adaptive LMS (TDLMS) Algorithm", IEEE Trnsactions on Circuits and Systems, vol.35, No. 5, May 1988, pp. 485 - 494).

$$W(k,l)^{(n+1)} = W(k,1)^{(n)} + 2 \cdot \mu \cdot e(m,n) \cdot X(m-k,n-l) \quad (6)$$

$k = -1, 0, 1$ $l = -2, -1, 0, ..., 2$

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where, μ shows a convergence coefficient (> 0), and $W(k,1)^{(n)}$ shows it to be the tap coefficient in the nth iteration.

In the circuit, the above equation is realized by D-FF, multiplier, and adder by each coefficient. In the actual circuit, $W(k,1)^{(n)}$ is multiplied by α, but it is in order to improve stability of the circuit. The coefficient $(2^{*}\mu)$ in the second term is replaced by β .

$0 < \alpha \leq 1, (2^{*} \mu) = \beta$ (7)

By the above construction, the wave interference from the adjacent track can be suppressed, and, in case of narrowing the track pitch, reproduced data error rate by cross talk can be reduced. Also, there can be realized a blind equalizer block and an optical disk recording/reproducing apparatus using such a blind equalizer block in which the interference fluctuation attributed to linear recording density, recording power irregularity, light spot, tracking error, etc. is automatically compensated to suppress such fluctuation.

Next, the second embodiment of the blind equalizer block with which the signal to noise ratio can be improved in comparison with the first embodiment is described.

Fig. 12 is a circuit diagram of an equalizer of the second embodiment of the blind equalizer block, and Fig. 13 is a circuit diagram of the coefficient control circuit of the second embodiment of the blind equalizer block.

In Fig. 12, 141 - 145, 155 - 159, 170 - 174 and 187 - 189 are D-FFs, 146 - 150, 160 - 164, 175 - 179, 190 and 191 are multipliers, 151 - 154, 165 - 169, 180 - 184, 192 and 193 are adders, 186 is a comparator, and 185 and 194 are subtractors. 271 is a sign detector. The sign detector 271 is composed of a subtractor 185 and a comparator 186, and its output is represented by a(m, n). The part 272 is a finite impulse response (FIR) low-pass filter. The FIR low-pass filter 272 is composed of D-FFs 187 - 189, multipliers 190 and 191, and adders 192 and 193, and performs band limitation of the output signal a(m, n) of the sign detector 271. The coefficient of the multipliers 190 and 191 is ϵ ($\epsilon > 0$).

In this embodiment, in order to improve the signal to noise ratio, the interference condition in the track is loosened and an FIR low-pass filter for band limitation is inserted after the output a(m, n) of the sign detector 271, the desired signal d(m, n) is set, as follows:

$d(m, n) = \epsilon^{*} a(m, n-1) + a(m, n) + \epsilon^{*} a(m, n+1)$ (8) where, $\epsilon > 0$.

By the above construction, the wave interference from the adjacent track can be suppressed, and, in case of narrowing the track pitch, reproduced data error rate by cross-talk can be reduced. Also, the interference fluctuation attributed to linear recording density, recording power irregularity, light spot, tracking error, etc. is automatically compensated to suppress such fluctuation. Also, there can be realized a blind equalizer block which improves the signal to noise ratio in comparison with the first embodiment of the blind equalizer block and an optical disk recording/reproducing apparatus using such blind equalizerblock.

In the case of the DBF which is the control system of the current optical disk, the reproduced clock timing error in recording and reproducing requires to be strictly controlled, because of a large problem of fluctuation of the circuit in the optical head 1 (eg., when, as in the magneto-optical disk apparatus, the reproduction circuit of the clock pit and the reproduction circuit of the magneto-optical data unit are different, the delay time of each circuit becomes irregular or temperature change may be produced).

However, according to the adaptive tap coefficient matrix compensation of the blind equalizer block, it is to perform an operation to provide the equalizer approximately with a delay characteristic according to the condition of recording and reproducing, so that it is possible to scheme this improvement. In the first and the second embodiment of the blind equalizer block, the equalizer is a T-spaced linear equalizer, so that the effect of this delay compensation is small. Accordingly, by constituting a T-2 spaced linear equalizer for the reproduced clock as the third embodiment of the blind equalizer block, this delay compensation effect can be rapidly increased. (cf. Literature: J. G. Proakis, "Digital Communications", second edition, McGraw-Hill, 1989).

Fig. 14 shows a circuit diagram of an equalizer of the blind equalizer block of the third embodiment, and Fig. 15 (a). and (b) show the circuit diagrams of the coefficient control circuit of the blind equalizer block of the third embodiment.

In Fig. 14, 274 - 282, 300 - 308, 327 - 335 and 356 - 360 are D-FFs, 283 - 291, 309 - 317, 336 - 344 and 361 - 364 are multipliers, 292 - 299, 318 - 326, 345 -353and 365 - 368 are adders. The equalization unit has a construction of 3 X 9 taps so as to doubly increase the clock frequency. 355 is comparator, and 354 and 369 are subtractors. 273 is a clock generator. 507 is a sign detector. The sign detector 507 is composed of a subtractor 354 and a comparator 355, and its output is represented by a(m, n) . 508 is a FIR low-pass filter. The FIR low-pass filter 508 is composed of D-FFs 356 - 360, multipliers 361 - 364 and adders 365 - 368, and performs band limitation of the output signal a(m, n) of the sign detector 507. The coefficient of the multipliers 361 and 364 is η ($\eta > 0$), and the coefficient of the multipliers 362 and 363 is ζ - ($\zeta > 0$) . The FIR low-pass filter 508 also has 5-tap construction so as to doubly increase the clock

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frequency.

In Fig. 15 (a), the parts 370 - 416 are multipliers, 417 - 431 are adders, 432 - 446 are D-FFs. In rig. 15 (b) , the parts 447 - 482 are multiplirs, 483 - 494 are adders, and 495 - 506 are D-FFs. The coefficient control circuits of Fig. 15 (a) and (b) are the circuits for changing over the coefficient matrix W(k, l) of the 3 X 9 taps of the equalization circuit of Fig. 14.

In Fig. 14, the clock generator 273 causes to generate the clocks of twofold frequency from the reproducing clock of the phase locked loop circuit 7. The AD converter 23, RAMs 24, 25, D-FF in Fig. 14, and D-FFs in Figs. 15 and 16 use the signal of the clock generator as a sampling clock. In order to give an effect similar to that of the equalizer of the second blind equalizer block, the number of taps of the qualizer is 9 taps, and the output y(m, n) of the equalizer is:

$$y(m, n) = \sum_{k=-1}^{1} \sum_{l=-4}^{4} W(k, l) \cdot X(m - k, n - l) \quad (9)$$

Also, each coefficient W(k, l) of the coefficient control circuit in Fig. 15 (a) and (b) is represented by the following equation:

$W(k,l)^{(n+1)} = W(k,l)^{(n)} + 2 \cdot \mu \cdot e(m,n) \cdot X(m-k,n-l)$ (10)

$k = -1, 0, 1$ $l = -4, -3, ..., 4$

where, μ shows a convergence coefficient (> 0).

In the actual circuit, $W(k,l)^{(n)}$ is multiplied by α, but it is in order to improve stability of the circuit. The coefficient $(2 \cdot \mu)$ in the second term is replaced by β.

$0 < \alpha \leq 1$, $(2 \cdot \mu) = \beta$ (11)

Further, the desired signal d(m, n) which is an output signal of the FIR low-pass filter 508 for band limitation of the sign detector 507 is set, as follows: $d(m, n) = \zeta \cdot a(m, n-2) + \eta \cdot a(m, n-1) + a(m, n) + \eta \cdot a(m, n+1) + \zeta \cdot a(m, n+2)$ (12)

where, η , $\zeta > 0$.

By the above construction, a T/2 spaced linear equalizer block for the reproduced clock can be realized.

By the abovementiioned constructiion, the wave interference from the adjacent track can be suppressed, and, in case of narrowing the track pitch, reproduced data error rate by cross-talk can be reduced. Also, the interference fluctuation attributed to linear recording density, recording power irregularity, light spot, tracking error, etc. is automatically compensated to suppress such fluctuation. Also., there can be realized a blind equalizer block which can automatically efficiently compensate the error of the clock timing and its fluctuation and an optical disk recording/reproducing apparatus using such blind equalizer block.

Claims

1. A data recording/reproducing appartus using a disk recording medium comprising:
recording/reproducing means for recording signals on and reproducing signals from the disk recording medium having formed thereon a plurality of tracks;
a servo-signal extractor for extracting a servo-signal from a first reproduced signal from said recording/reproducing means;
a clock reproducer for extracting a reproducing clock from the first reproduced signal;
a switch for changing over the first reproduced signal and a second reproduced signal from said recording/reproducing means;
an equalizer block for equalizing an output signal of said switch by two-dimensional equalizations in the longitudinal direction and the latitudinal direction of a track;
an address decoder for decoding an address signal from an output of said equalizer block; and
a controller for controlling said switch and said equalizer block using an output of said address decoder.

2. A data recording/reproducing appartus using a disk recording medium comprising:
an optical head for performing recording and reproducing for an optical disk having formed thereon a plurality of tracks;
a servo-signal extractor for extracting a servo-signal from a first reproduced signal from said optical head;

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a clock reproducer for extracting a reproducing clock from the first reproduced signal;
a switch for changing over the first reproduced signal and a second reproduced signal from said optical head;
an equalizer block for equalizing an output signal of said switch by two-dimensional equalizations in the longitudinal direction and the latitudinal direction of a track;
an address decoder for decoding an address signal from an output of said equalizerblock; and
a controller for controlling said switch and said equalizer block using an output of said address decoder.

3. An equalizer apparatus comprising:
an analog-digital converter for sampling, quantitizing and outputting a reproduced signal from a disk recording medium;
a memory for storing signal trains of a plurality of tracks outputted from said analog-digital converter; and
an equalizer for reading out simultaneously the signal trains of the plurality of tracks stored in said memory and performing equalization to either one of a wave interference in the longitudinal direction of a track and a wave interference from an adjacent track.

4. An equalizer apparatus according to Claim 3, wherein the sampling rate or the analog-digital converter is equal to the channel bit rate of the reproduced signal.

5. An equalizer apparatus comprising:
an analog-digital converter for sampling, quantitizing and outputting a reproduced signal from a disk recording medium;
a memory for storing signal trains of a plurality of tracks outputted from said analog-digital converter;
an equalizer for reading out simultaneously the signal trains of the plurality of tracks stored in said memory and performing equalization to either one of a wave interference in the longitudinal direction of a track and a wave interference from an adjacent track;
a sign detector for detecting the sign of a digital signal outputted from the analog-digital converter from an output of said equalizer; and
a coefficient control circuit for varying a characteristic of said equalizer so as to minimize errors of the output of said equalizer and an output of said sign detector.

6. An equalizer apparatus according to Claim 5, wherein the sampling rate of the analog-digital converter is equal to the channel bit rate of the reproduced signal.

7. An equalizer apparatus comprising:
an analog-digital converter for sampling, quantitizing and outputting a reproduced signal from a disk recording medium;
a memory for storing signal trains of a plurality of tracks outputted from said analog-digital converter;
an equalizer for reading out simultaneously the signal trains of the plurality of tracks stored in said memory and performing equalization to either one of a wave interference in the longitudinal direction of a track and a wave interference from an adjacent track;
a sign detector for detecting the sign of a digital signal outputted from the analog-digital converter from an output of said equalizer;
a Finite Impulse Response low-pass filter for low-passing an output of said sign detector; and
a coefficient control circuit for varying a characteristic of said equalizer so as to minimize errors of the output of said equalizer and an output of said Finite Impulse Response low-pass filter.

8. An equalizer apparatus according to Claim 7, wherein the sampling rate of the analog-digital converter is equal to the channel bit rate of the reproduced signal.

9. An equalizer apparatus according to Claim 7, wherein the sampling rate of the analog-digital converter is equal to twofold the channel bit rate of the reproduced signal.

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BNSDOCID: <EP 0375342A2_I_>

Neu eingereicht / Newly filed / Nouvellement déposé

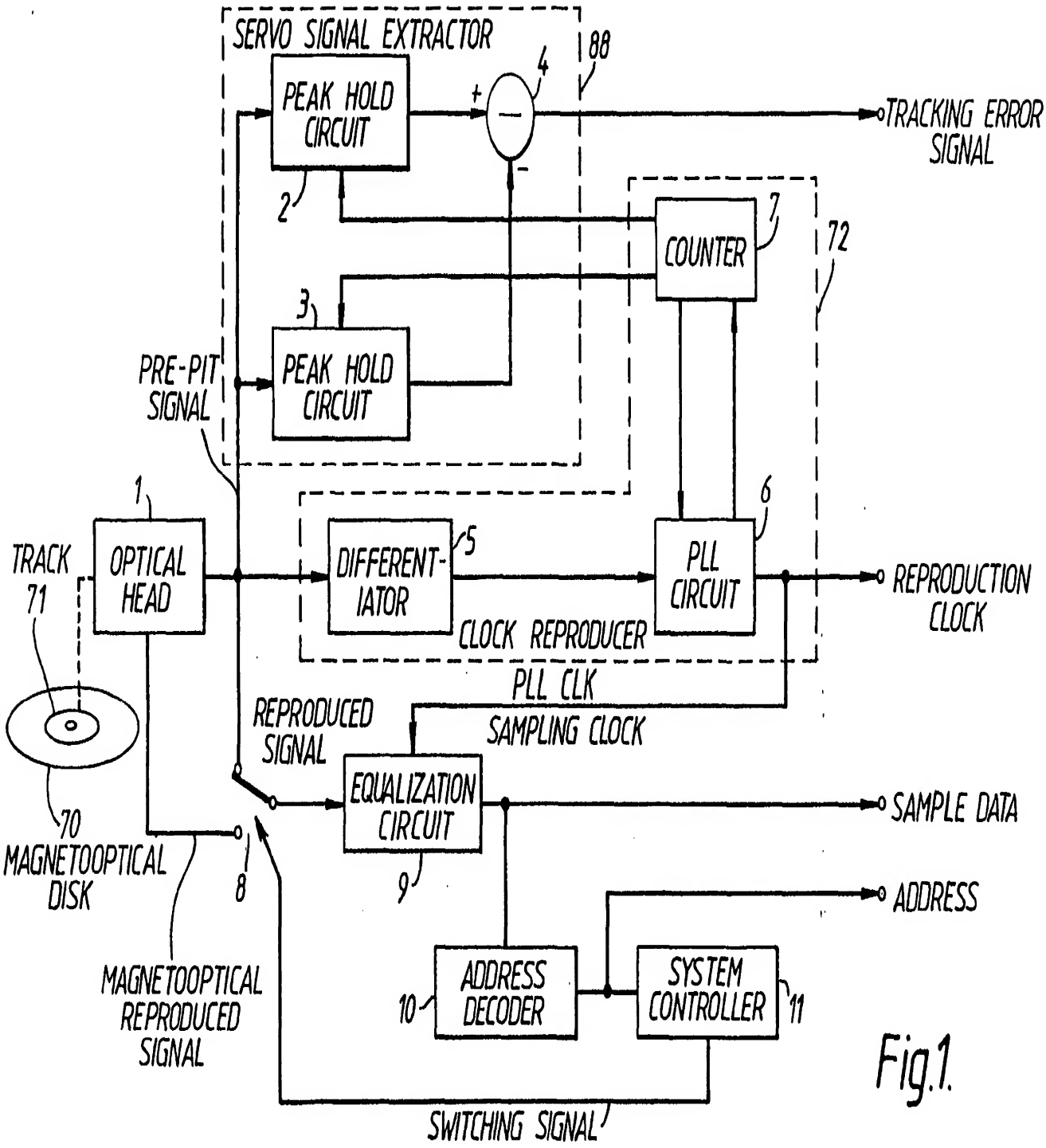

Fig.1.

BNSDOCID: <EP_____0375342A2_I_>

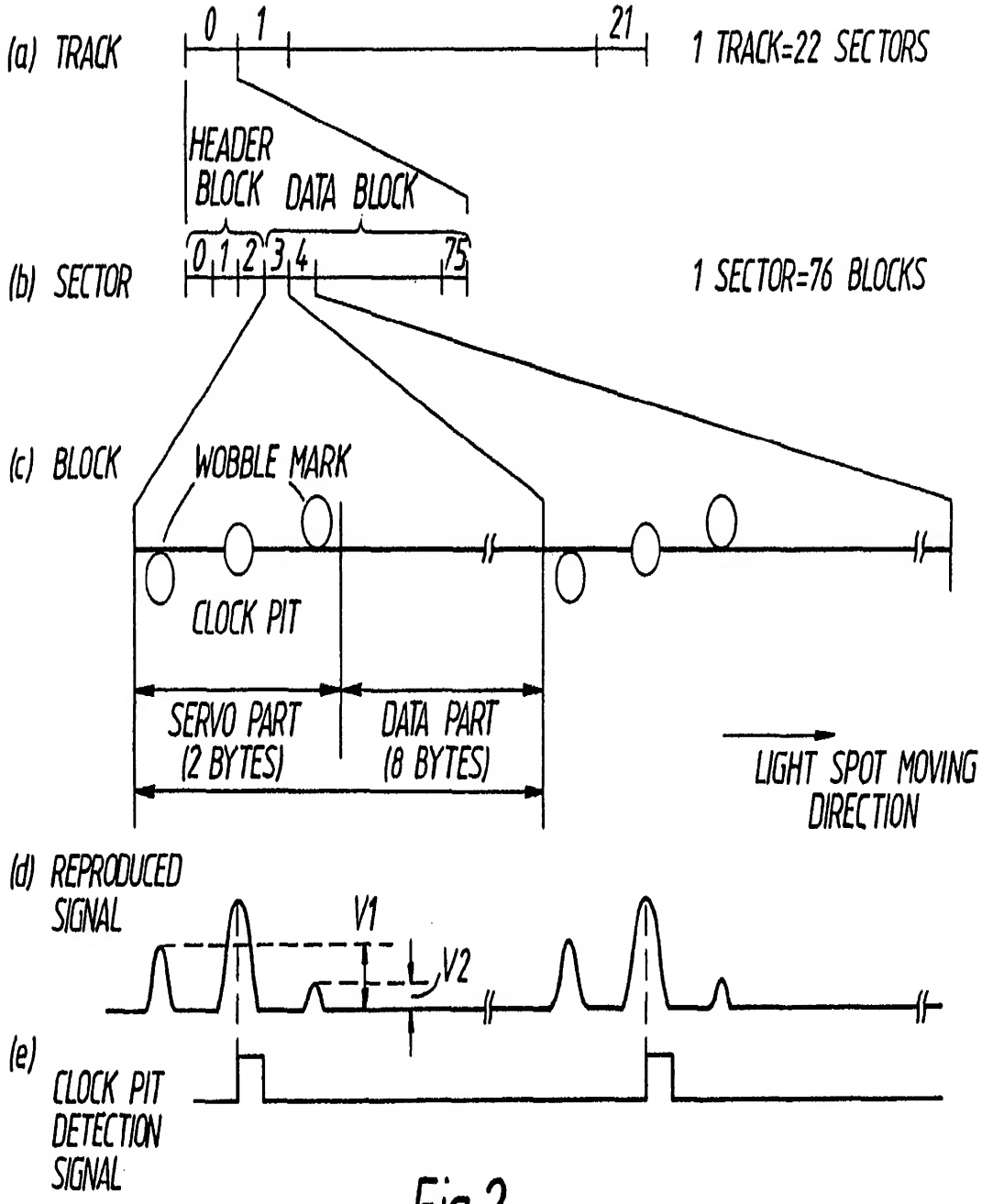

Fig.2.

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BNSDOCID: <EP_____0375342A2_I_>

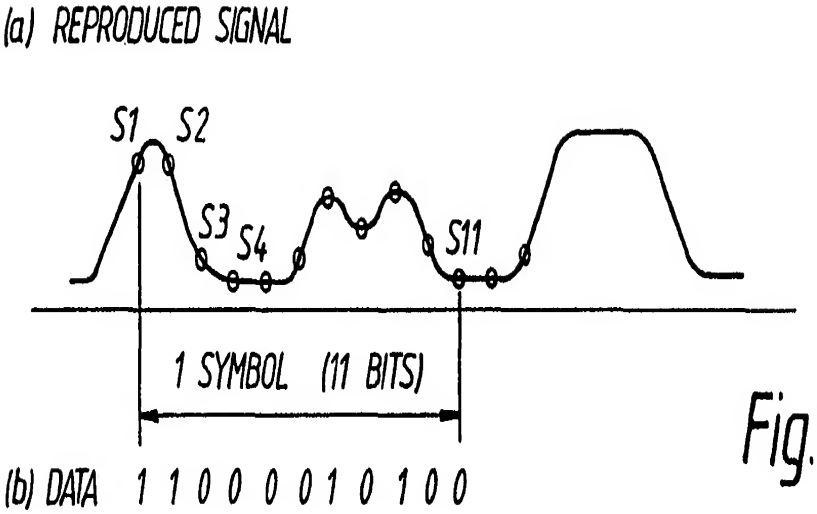

Fig.3.

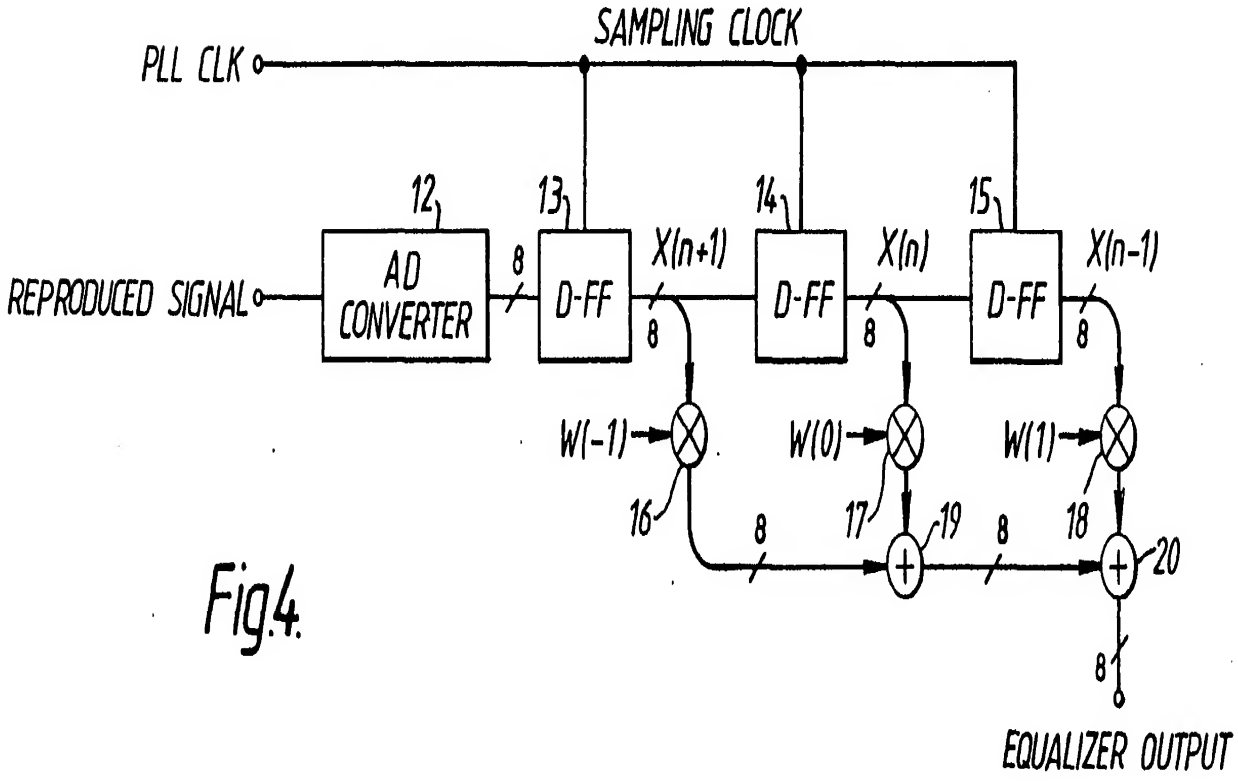

Fig.4.

EP 0 375 342 A2

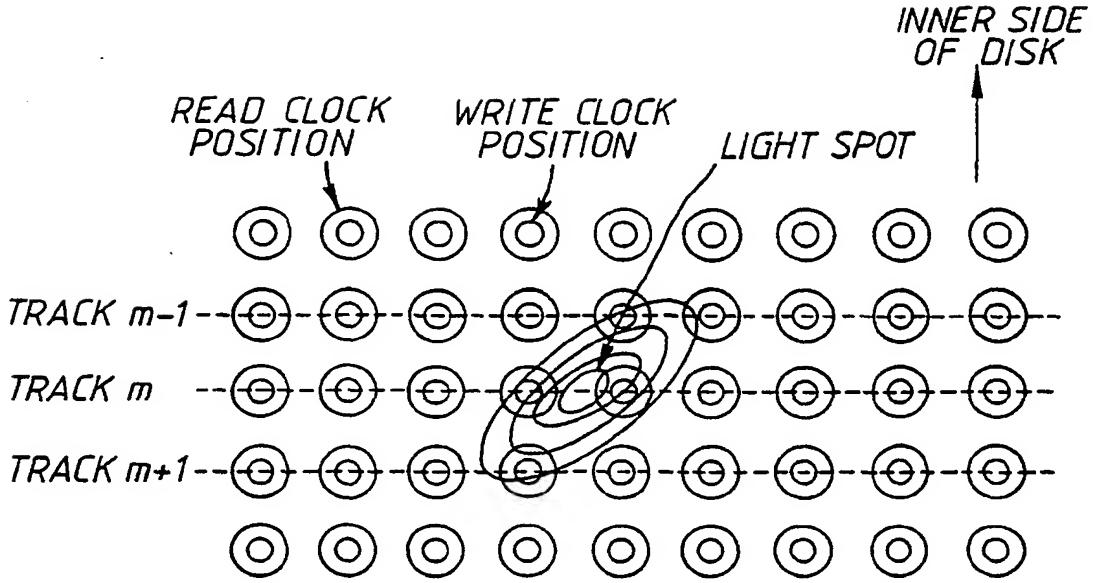
INNER SIDE OF DISK
READ CLOCK POSITION
WRITE CLOCK POSITION
LIGHT SPOT
TRACK m-1
TRACK m
TRACK m+1

Fig. 5.

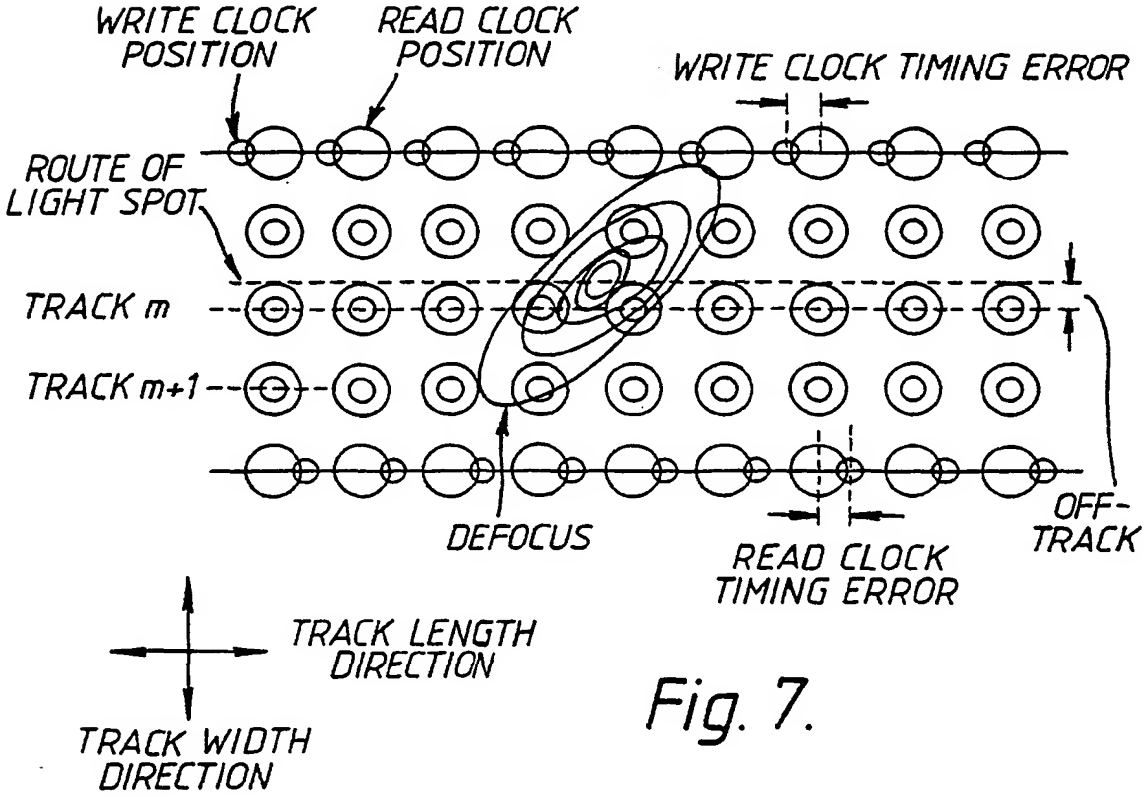
WRITE CLOCK POSITION
READ CLOCK POSITION
WRITE CLOCK TIMING ERROR
ROUTE OF LIGHT SPOT
TRACK m
TRACK m+1
DEFOCUS
READ CLOCK TIMING ERROR
OFF-TRACK
TRACK LENGTH DIRECTION
TRACK WIDTH DIRECTION

Fig. 7.

BNSDOCID: <EP 0375342A2_1_>

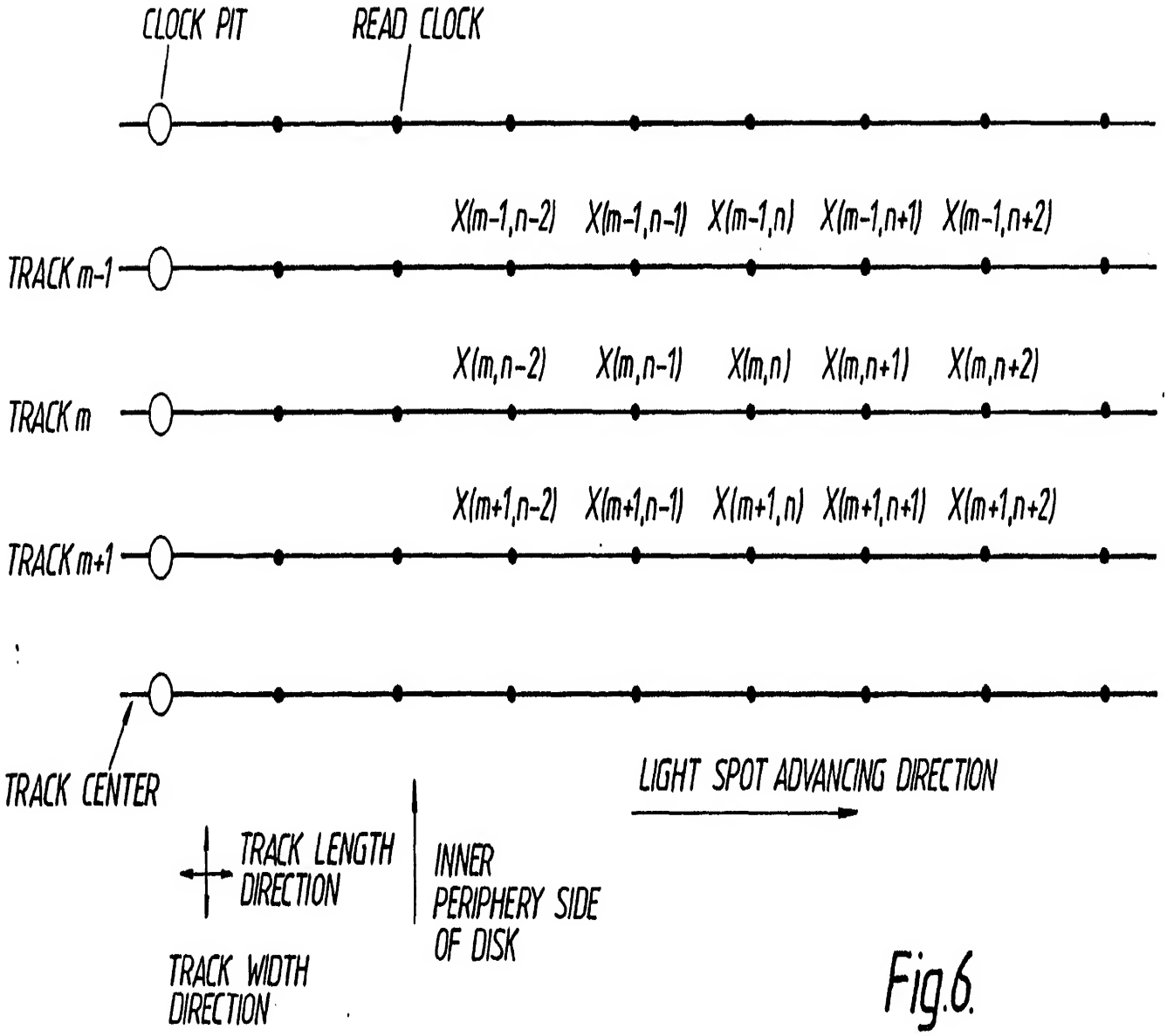

Fig.6.

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Neu eingereicht / N
Nouvellement c

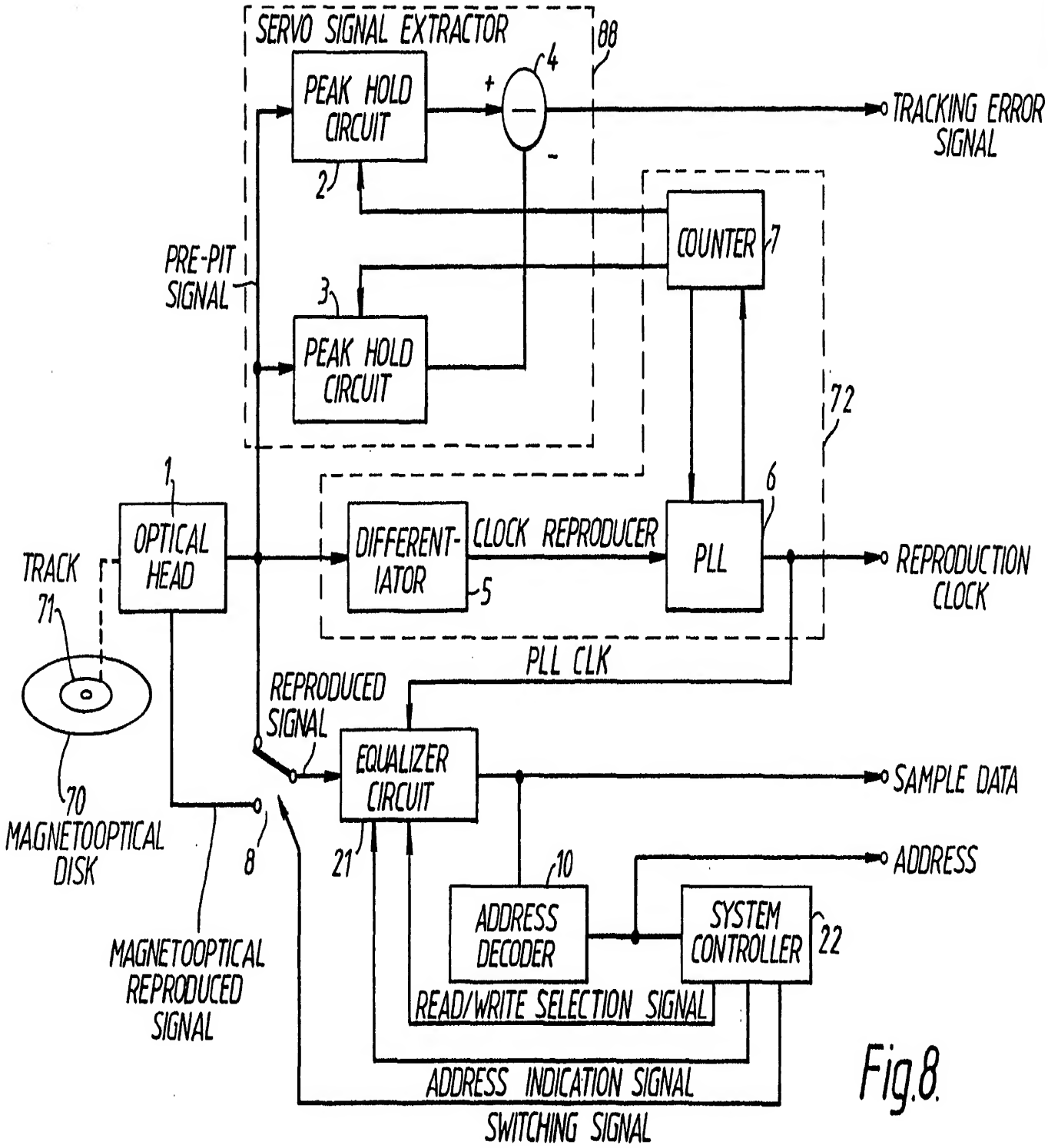

Fig.8.

Neu eingereicht / Newly filed
Nouvellement déposé

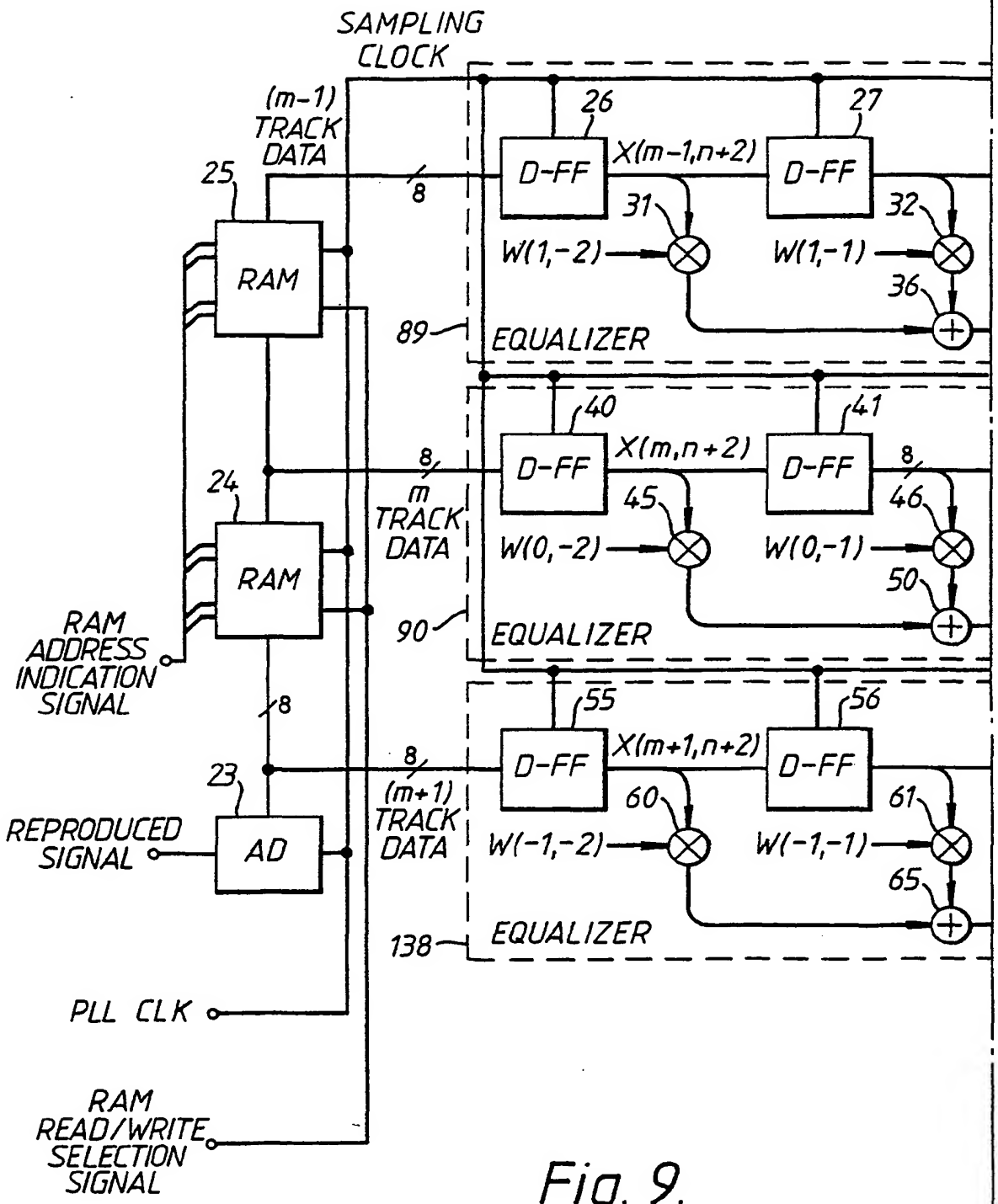

Fig. 9.

BNSDOCID: <EP_____0375342A2_I_>

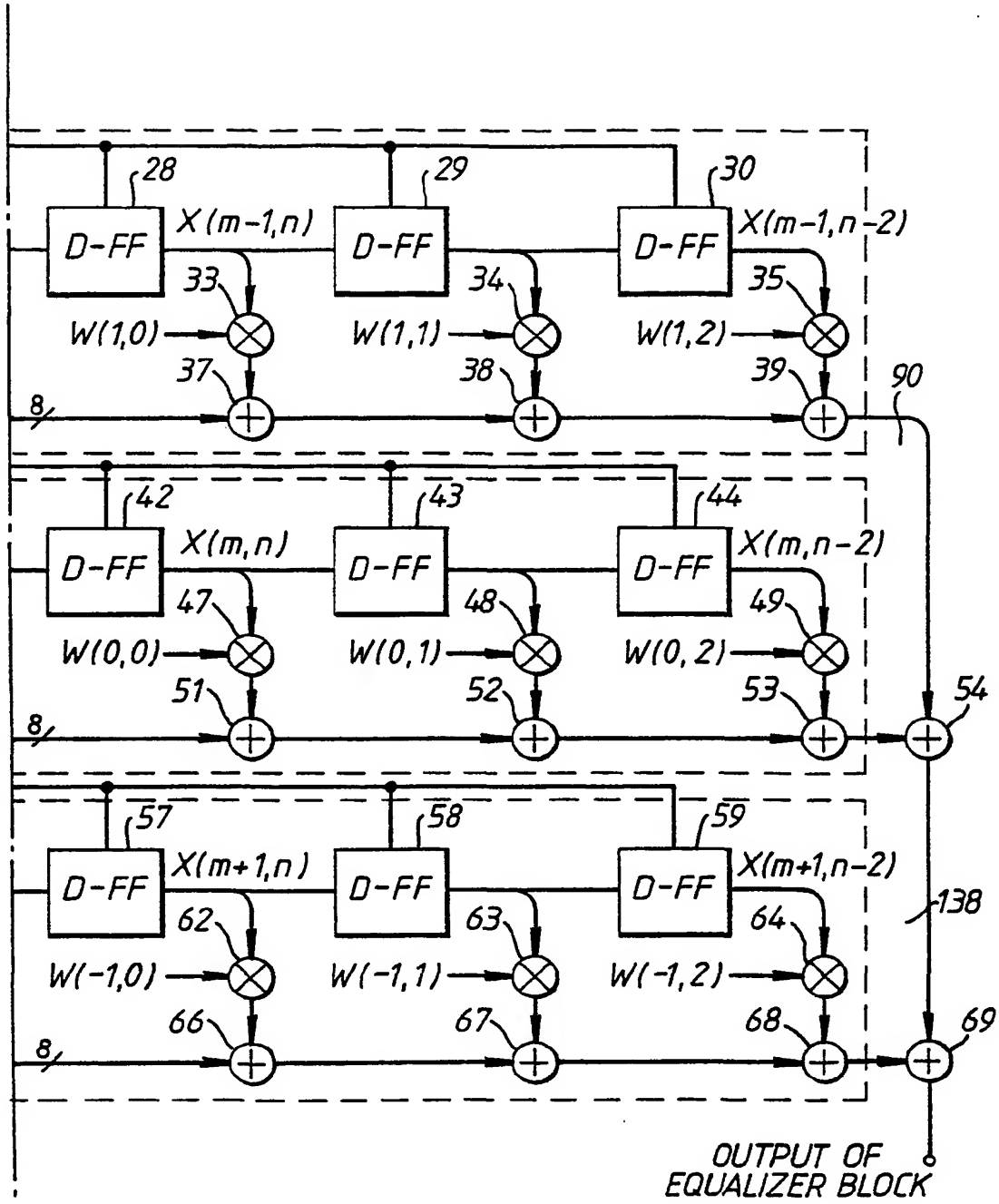

Fig. 9 (cont.)

BNSDOCID: <EP_____0375342A2_1_>

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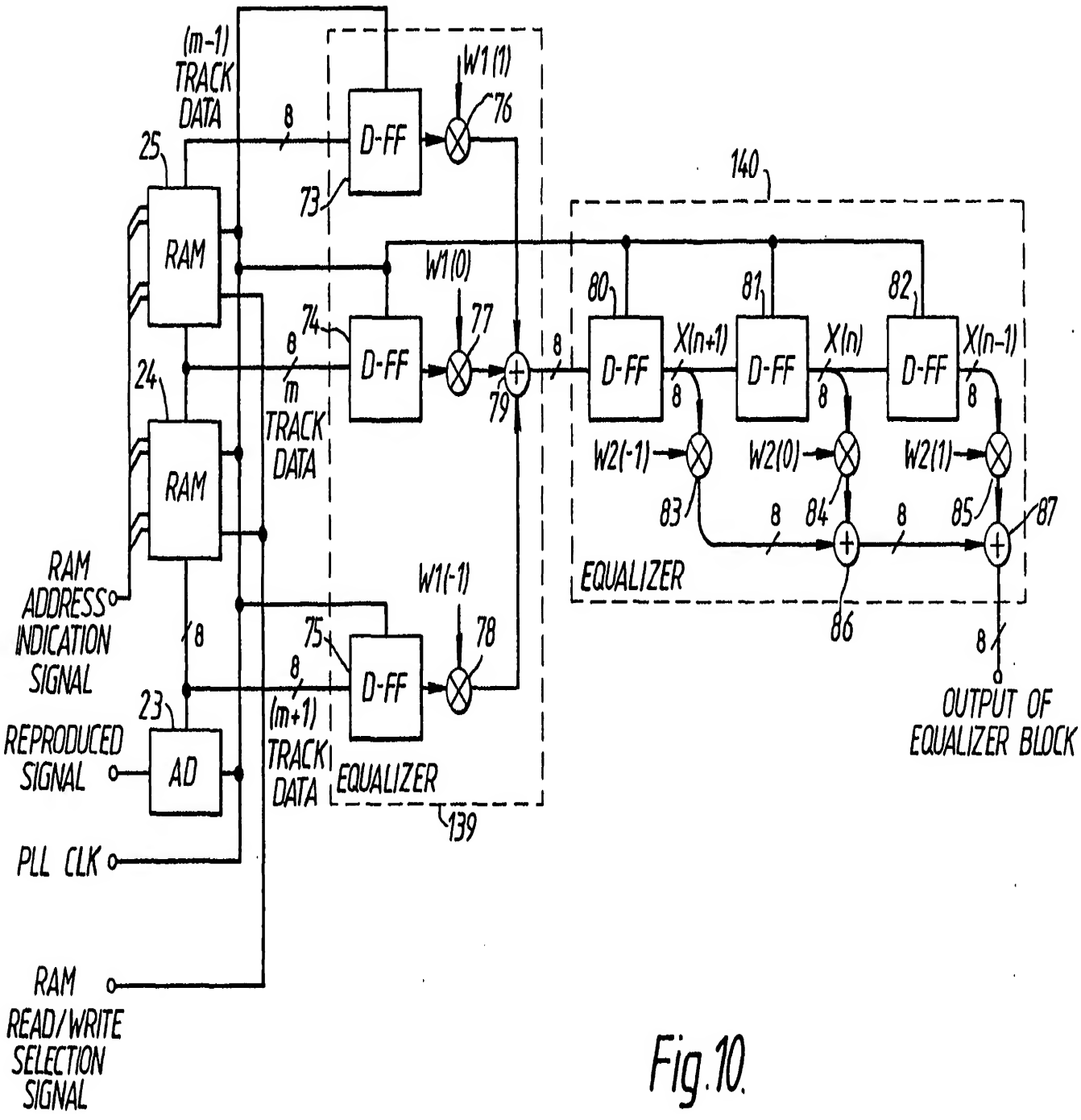

Fig.10.

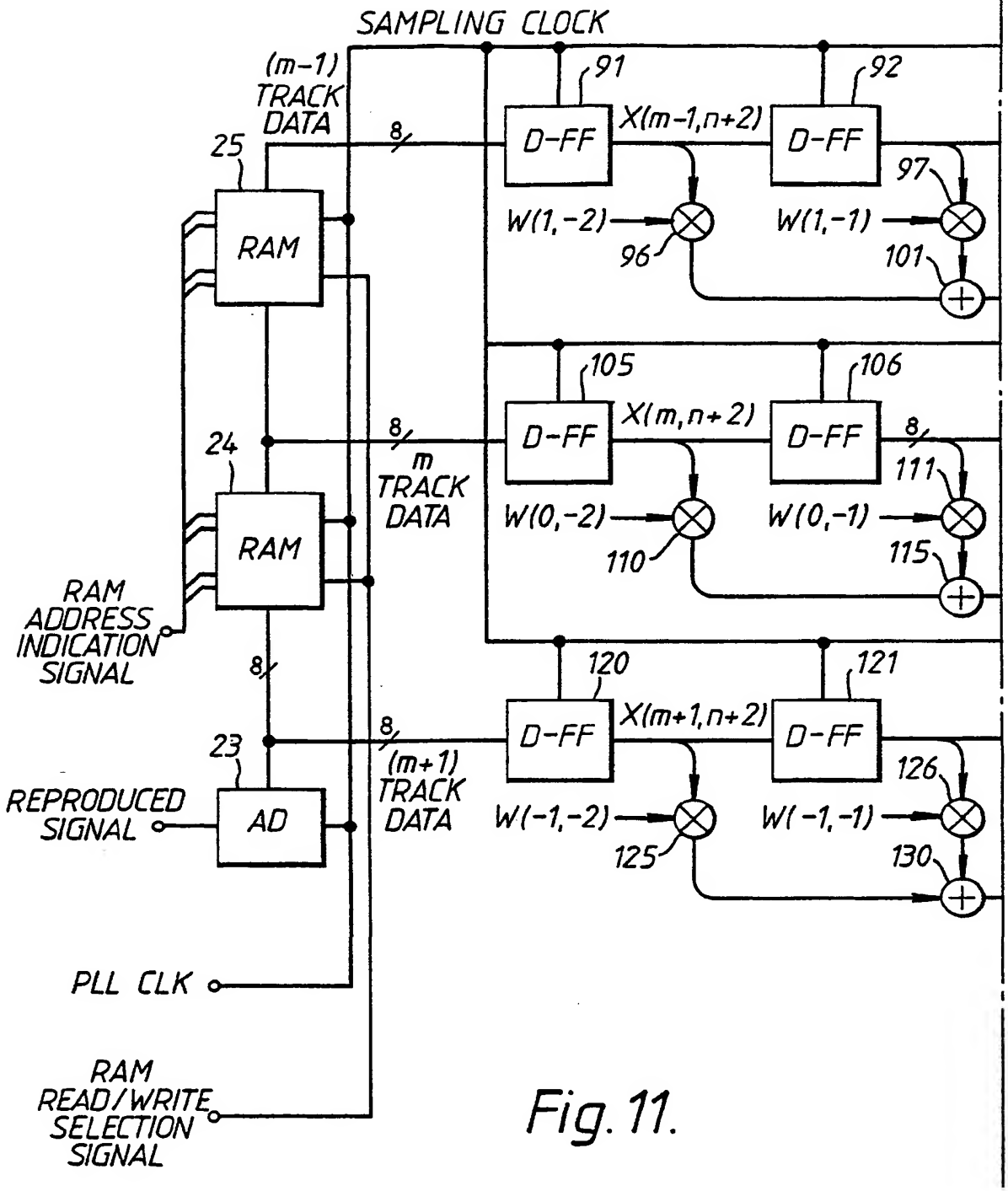
SAMPLING CLOCK
(m-1) TRACK DATA
8
25
RAM
24
RAM
m TRACK DATA
RAM ADDRESS INDICATION SIGNAL
8
23
AD
REPRODUCED SIGNAL
8
(m+1) TRACK DATA
PLL CLK
RAM READ/WRITE SELECTION SIGNAL
91
D-FF
X(m-1,n+2)
92
D-FF
97
W(1,-2)
96
W(1,-1)
101
105
D-FF
X(m,n+2)
106
D-FF
8
111
W(0,-2)
110
W(0,-1)
115
120
D-FF
X(m+1,n+2)
121
D-FF
126
W(-1,-2)
125
W(-1,-1)
130

Fig. 11.

Neu eingereicht / Newly
Neuvellement déposé

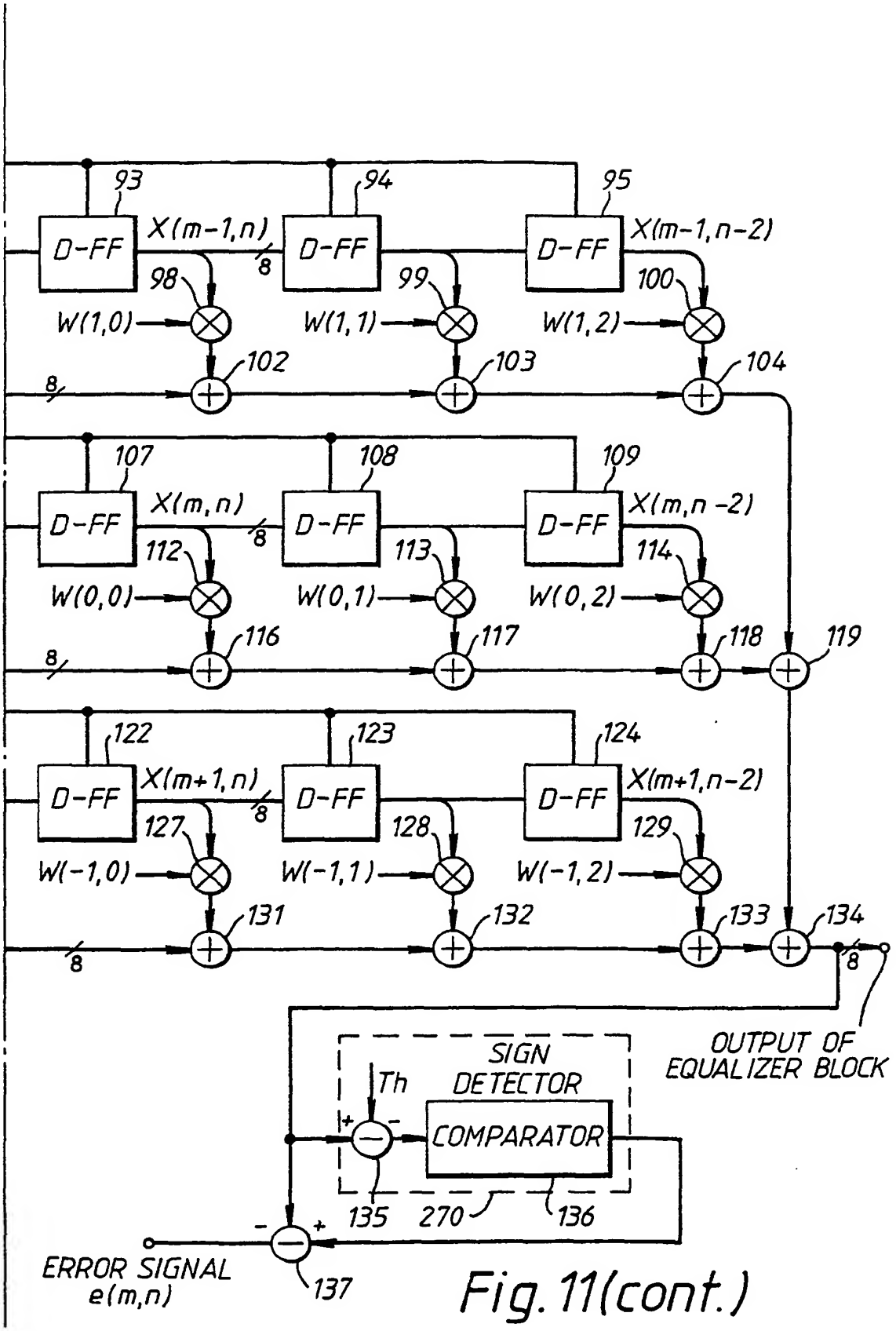

Fig. 11(cont.)

Neu eingereicht / Nouvellement déposé

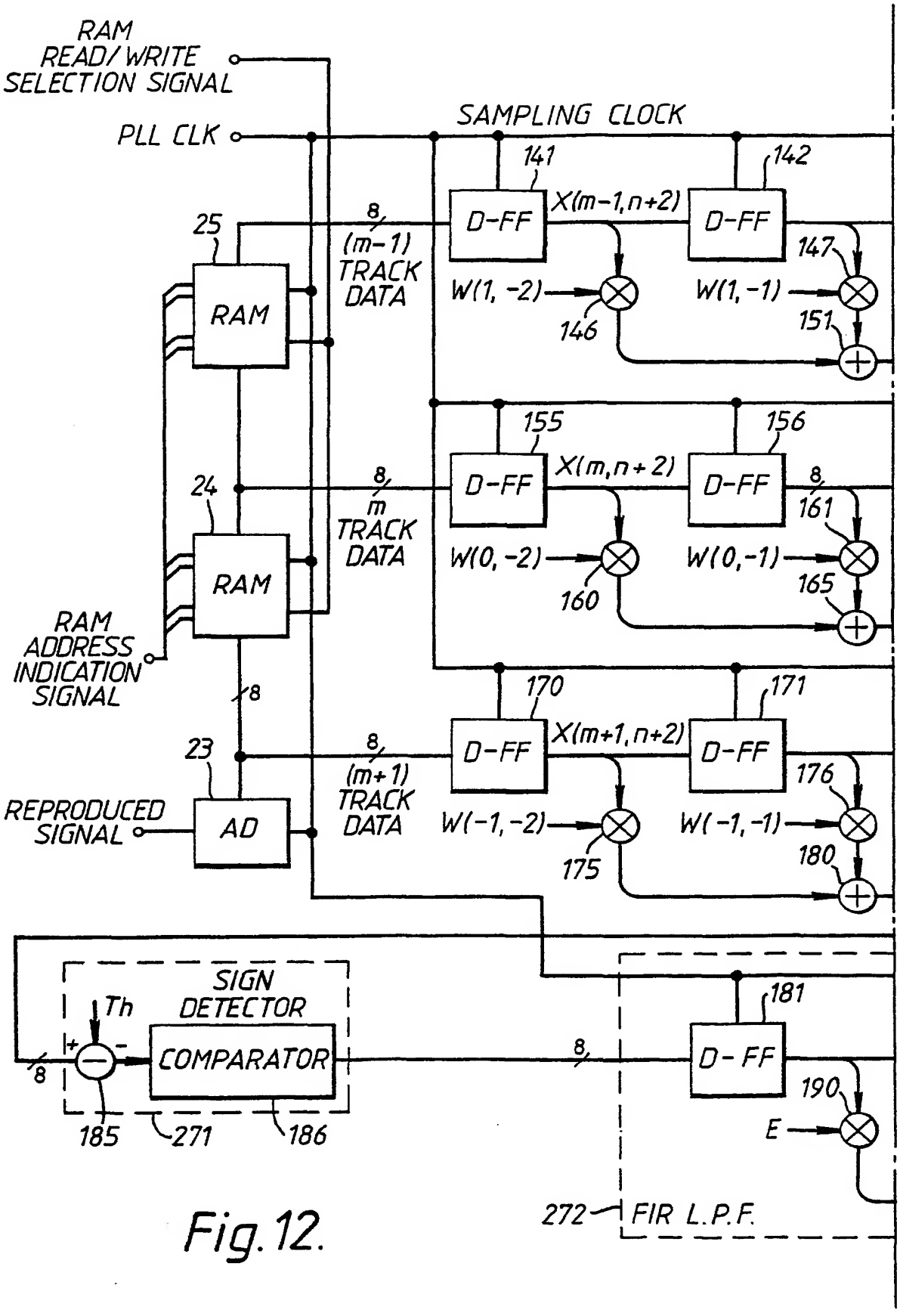

Fig. 12.

BNSDOCID: <EP_____0375342A2_I_>

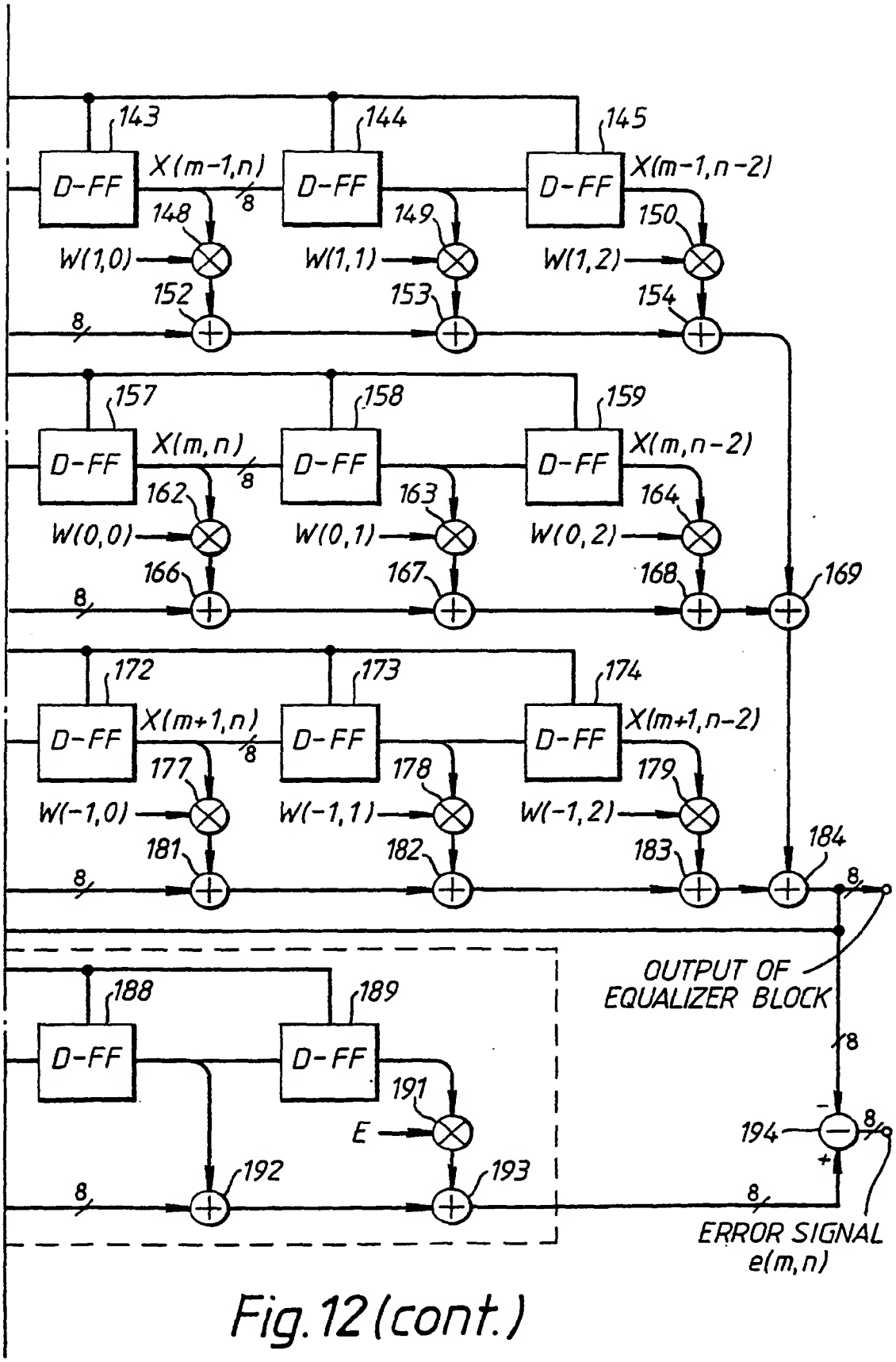

Fig. 12 (cont.)

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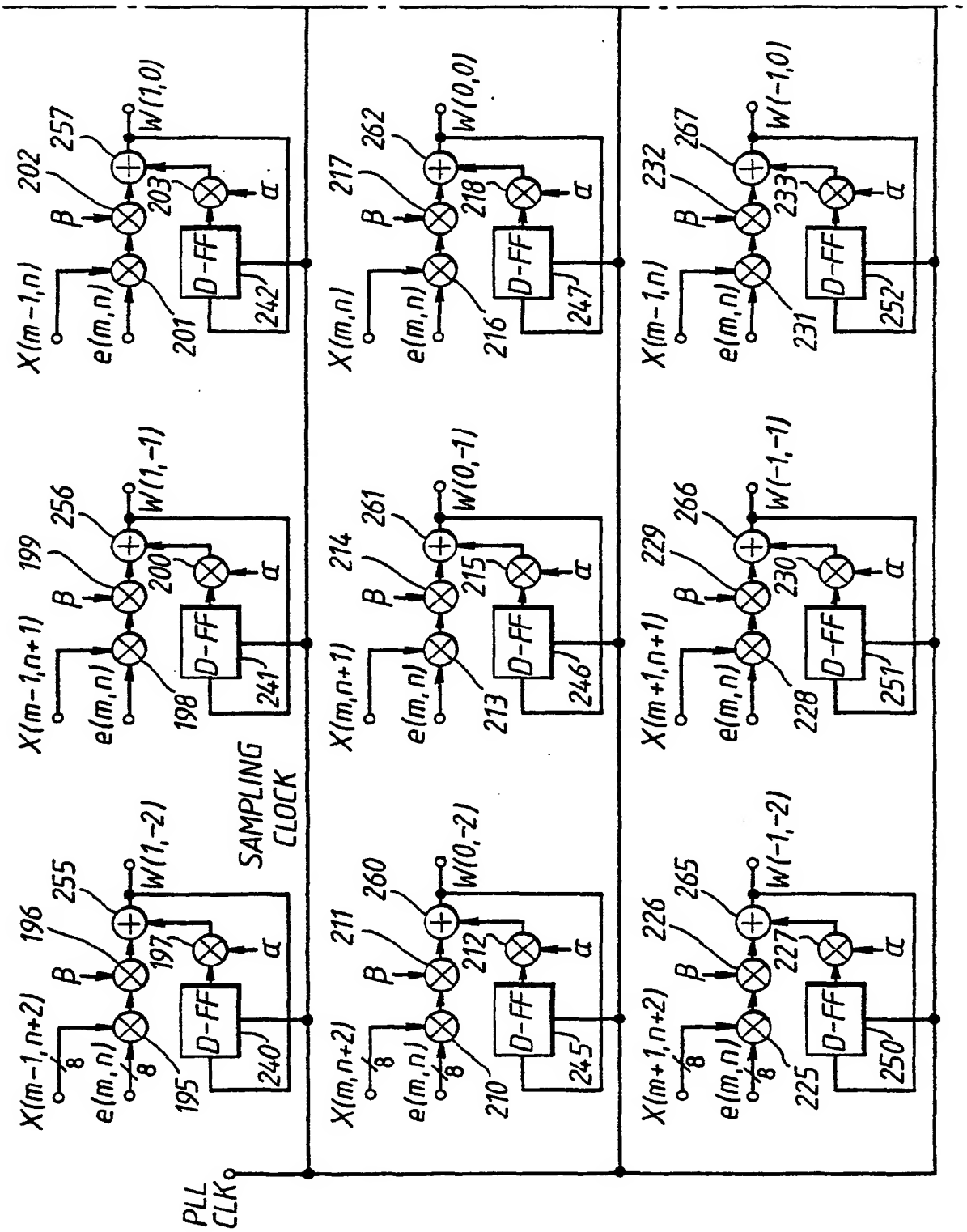

Fig. 13.

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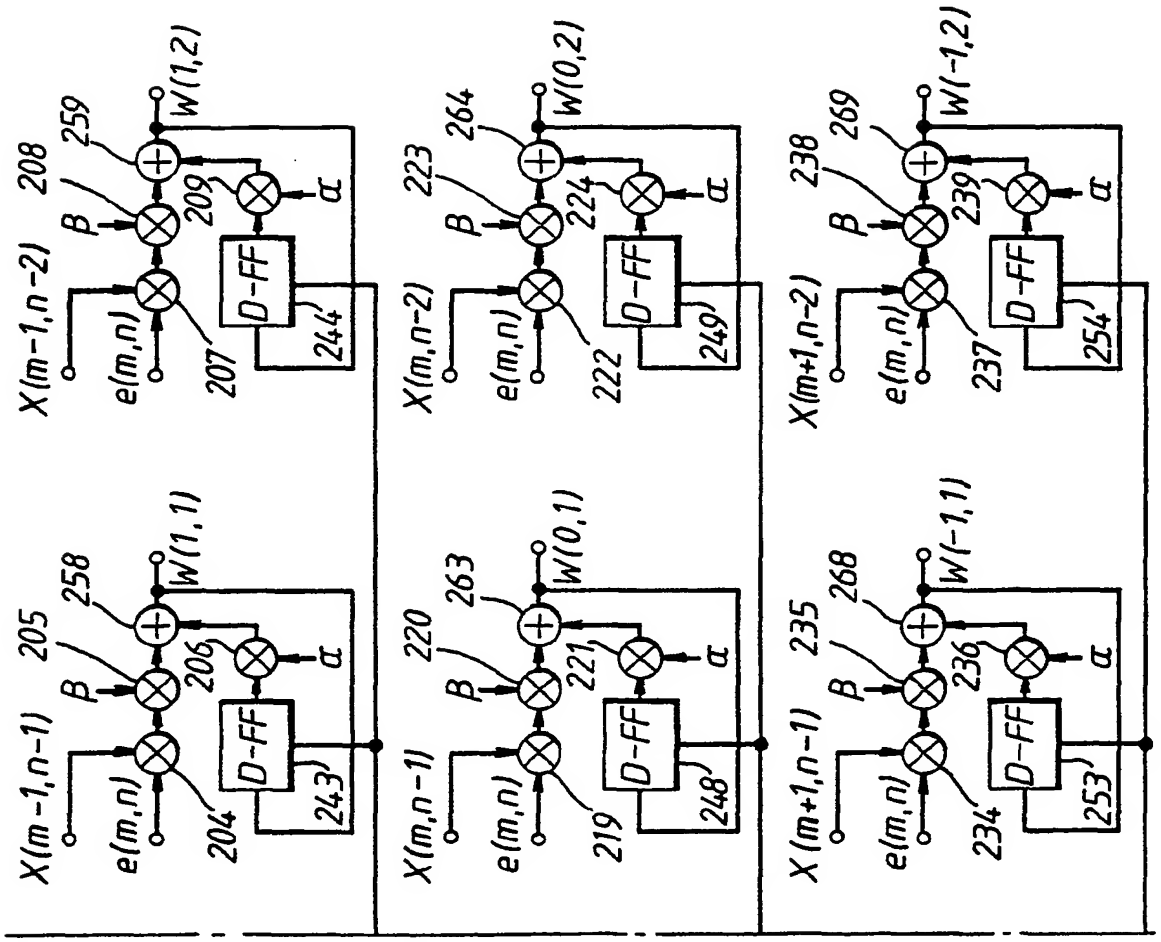

Fig.13(cont.)

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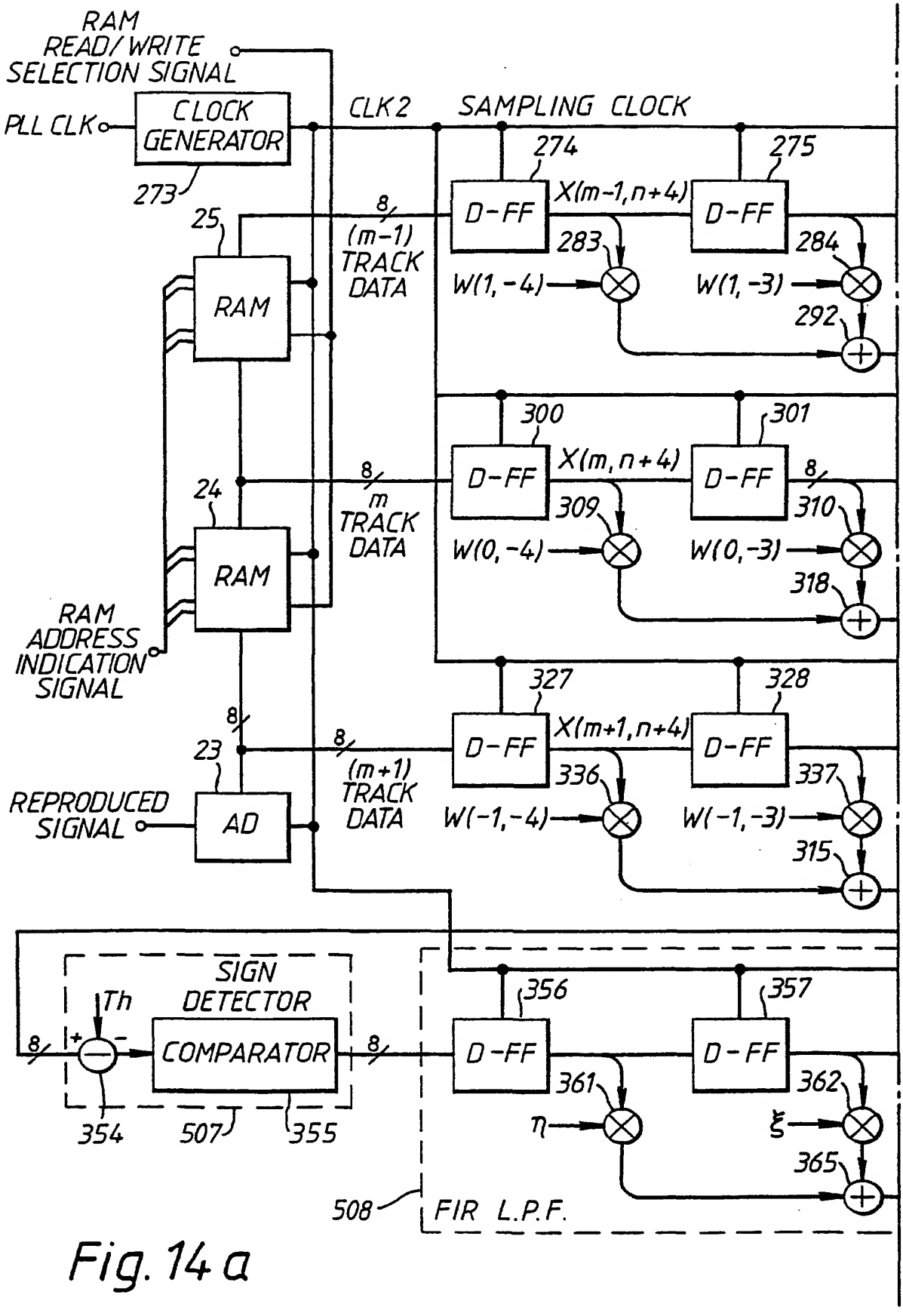

Fig. 14 a

BNSDOCID: <EP_____0375342A2_I_>

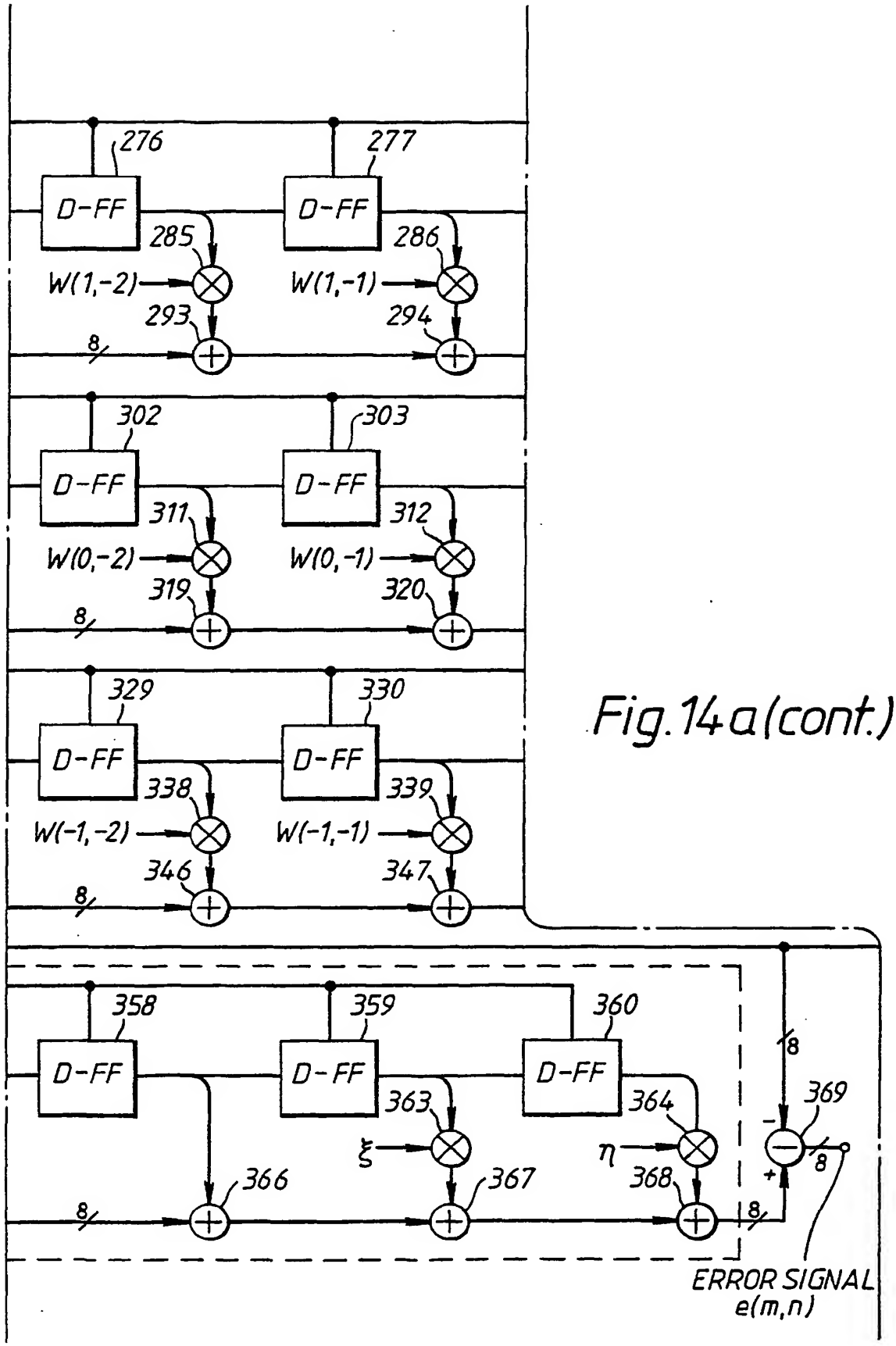
276
277
D-FF
D-FF
285
286
W(1,-2)
W(1,-1)
293
294
8
302
303
D-FF
D-FF
311
312
W(0,-2)
W(0,-1)
319
320
8
329
330
D-FF
D-FF
338
339
W(-1,-2)
W(-1,-1)
346
347
8
358
359
360
D-FF
D-FF
D-FF
363
364
369
ξ
η
366
367
368
8
8
8
ERROR SIGNAL
e(m,n)

Fig. 14a (cont.)

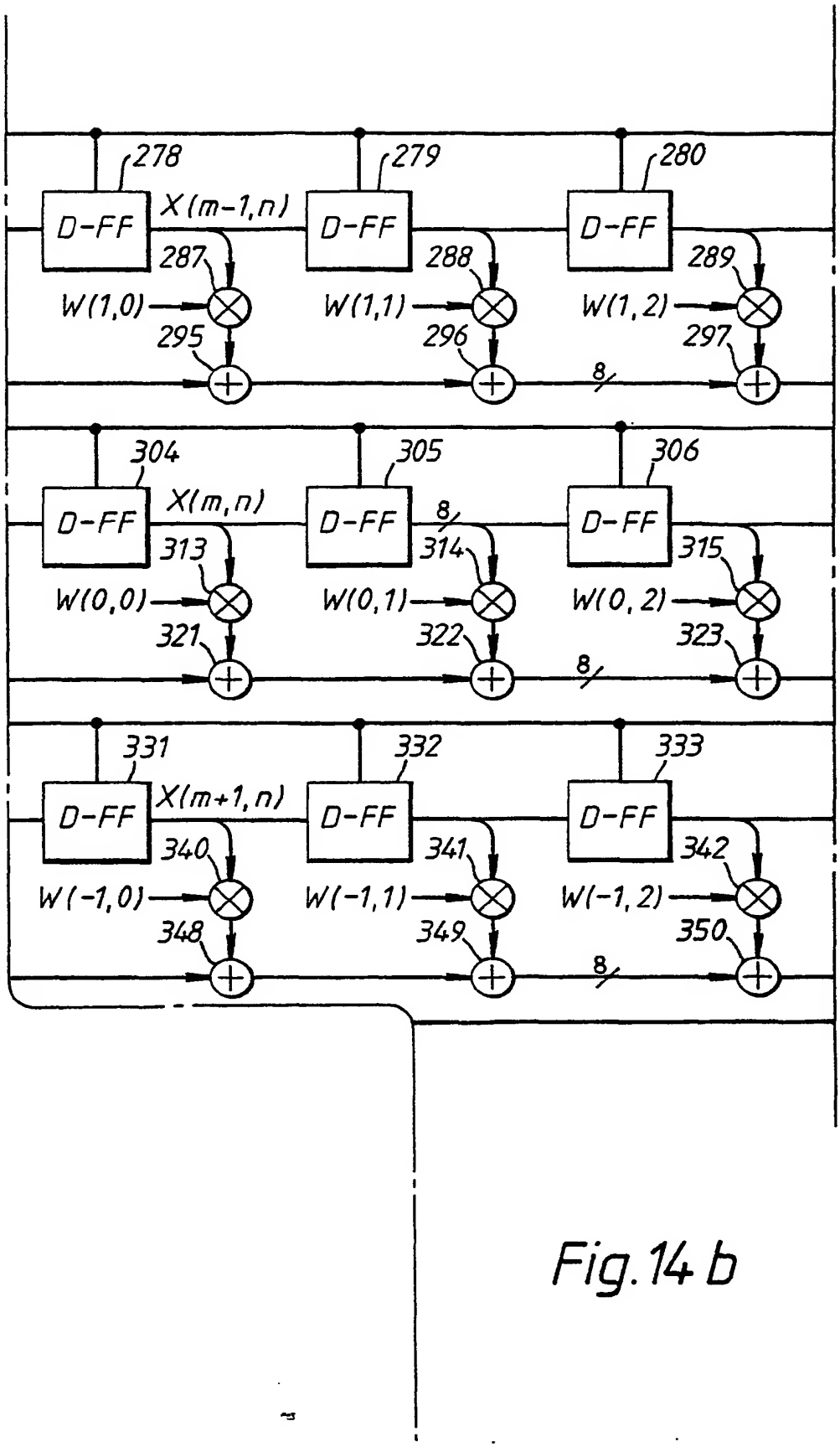
278
279
280
D-FF
D-FF
D-FF
X(m-1,n)
287
288
289
W(1,0)
W(1,1)
W(1,2)
295
296
297
8
304
305
306
D-FF
D-FF
D-FF
X(m,n)
8
313
314
315
W(0,0)
W(0,1)
W(0,2)
321
322
323
8
331
332
333
D-FF
D-FF
D-FF
X(m+1,n)
340
341
342
W(-1,0)
W(-1,1)
W(-1,2)
348
349
350
8

Fig. 14 b

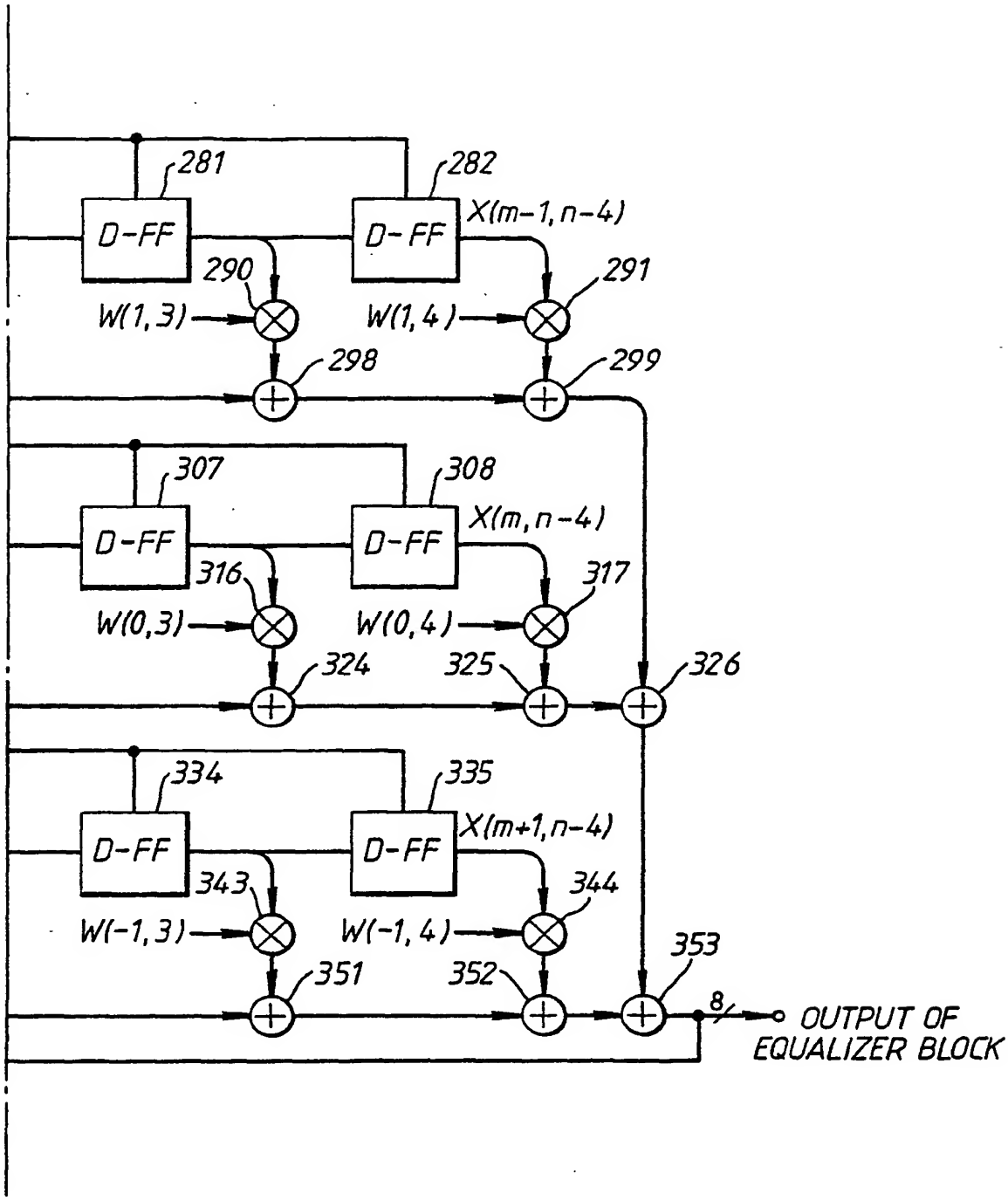
281
282
D-FF
D-FF
X(m-1,n-4)
290
291
W(1,3)
W(1,4)
298
299
307
308
D-FF
D-FF
X(m,n-4)
316
317
W(0,3)
W(0,4)
324
325
326
334
335
D-FF
D-FF
X(m+1,n-4)
343
344
W(-1,3)
W(-1,4)
351
352
353
8
OUTPUT OF EQUALIZER BLOCK

Fig. 14 b (cont.)

Neu eingereicht
Nouvellement déposé

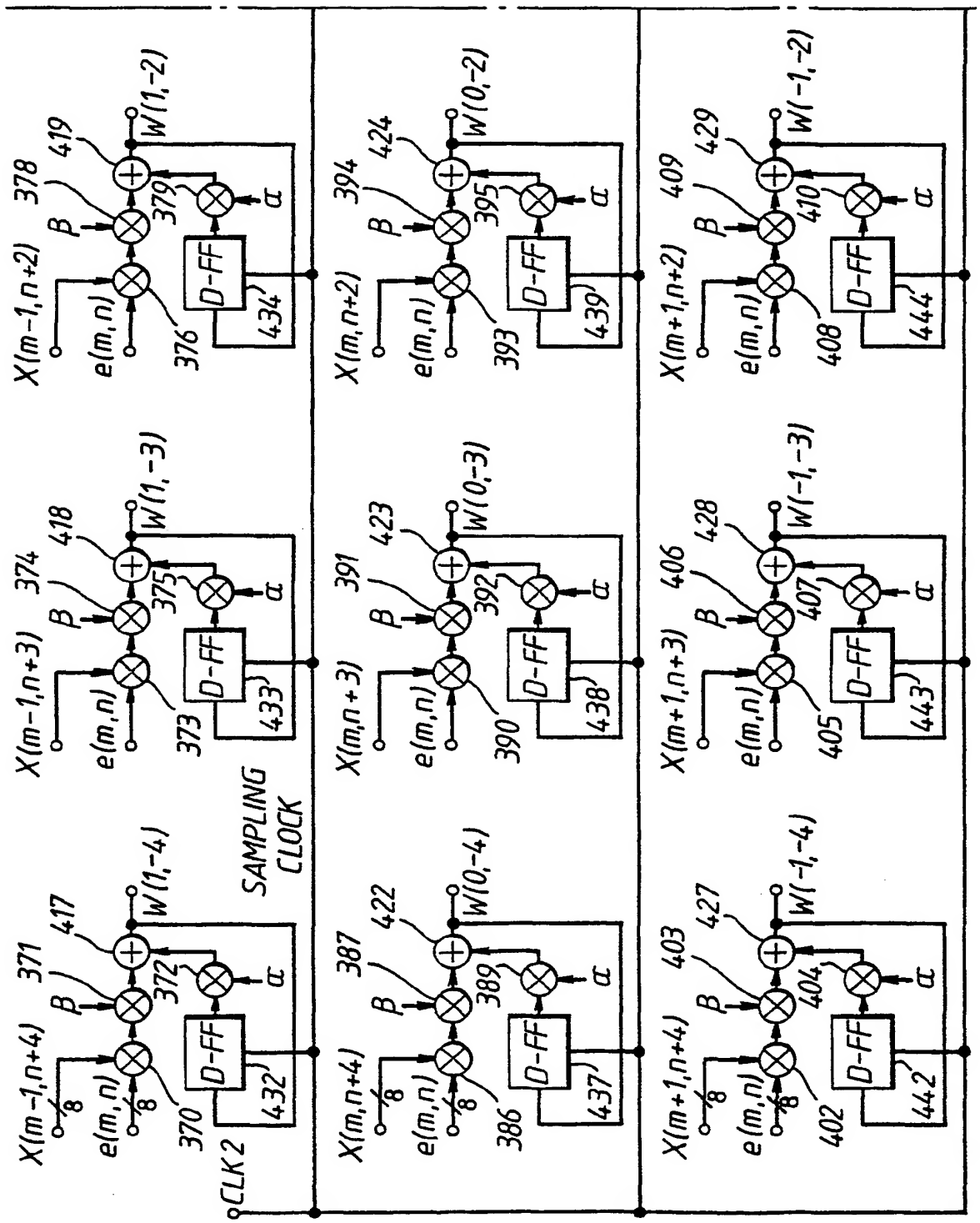

Fig. 15 a

BNSDOCID: <EP_____0375342A2_I_>

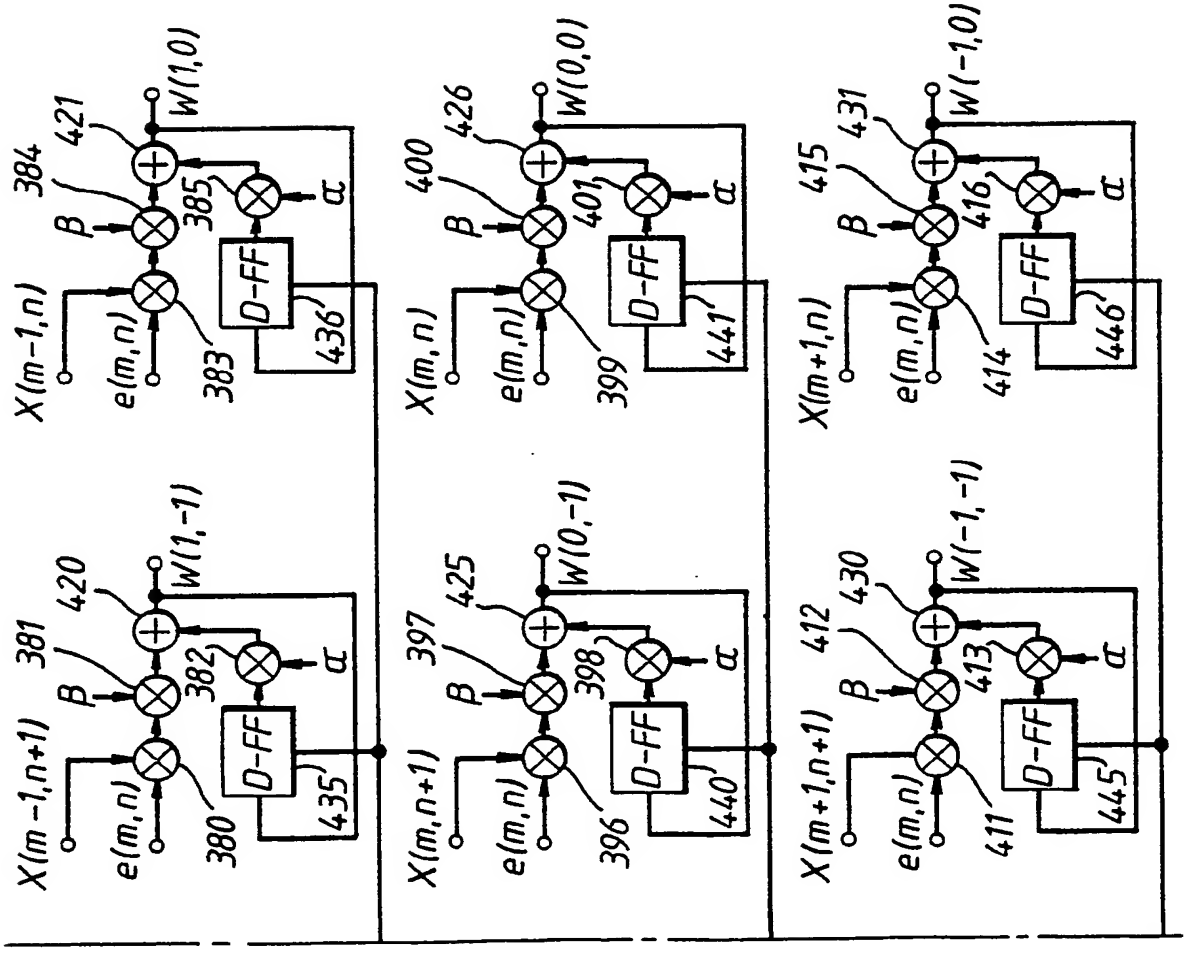

Fig.15 a (cont.)

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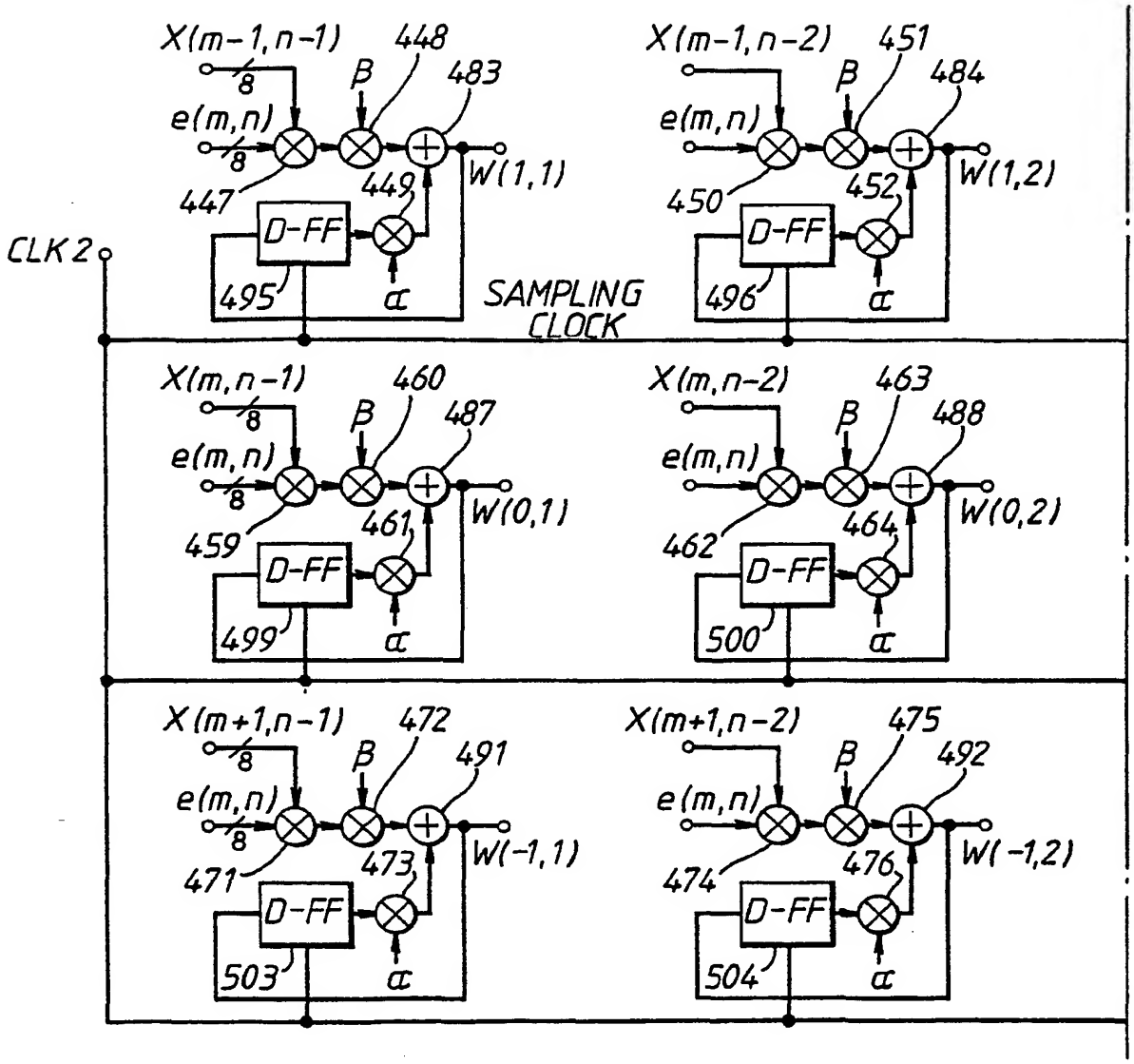
X(m-1,n-1)
448
483
e(m,n)
8
447
449
W(1,1)
D-FF
495
α
X(m-1,n-2)
451
484
450
452
W(1,2)
496
CLK2
SAMPLING CLOCK
X(m,n-1)
460
487
459
461
W(0,1)
499
X(m,n-2)
463
488
462
464
W(0,2)
500
X(m+1,n-1)
472
491
471
473
W(-1,1)
503
X(m+1,n-2)
475
492
474
476
W(-1,2)
504
β

Fig.15 b

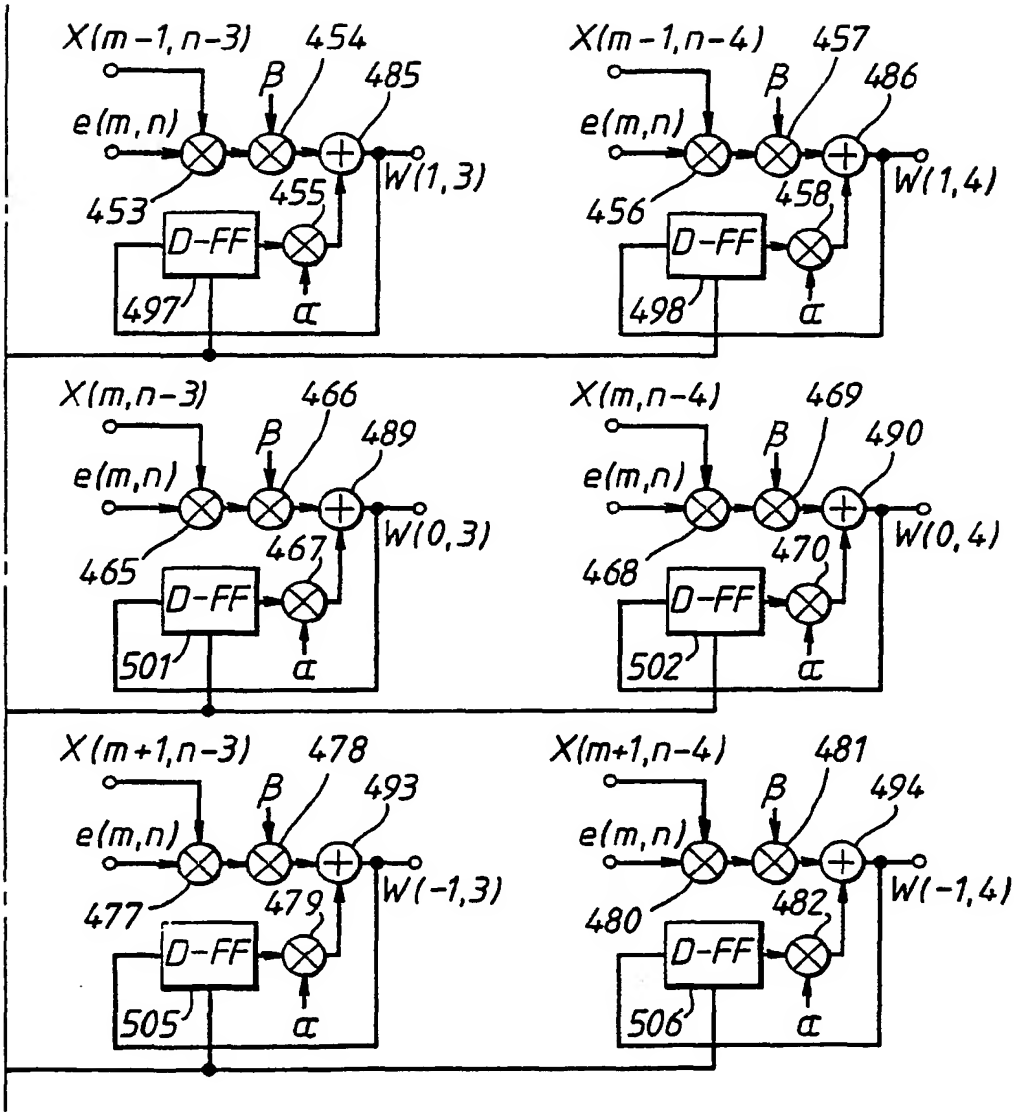
X(m-1,n-3)
454
β
485
e(m,n)
W(1,3)
453
455
D-FF
497
α
X(m-1,n-4)
457
β
486
e(m,n)
W(1,4)
456
458
D-FF
498
α
X(m,n-3)
466
β
489
e(m,n)
W(0,3)
465
467
D-FF
501
α
X(m,n-4)
469
β
490
e(m,n)
W(0,4)
468
470
D-FF
502
α
X(m+1,n-3)
478
β
493
e(m,n)
W(-1,3)
477
479
D-FF
505
α
X(m+1,n-4)
481
β
494
e(m,n)
W(-1,4)
480
482
D-FF
506
α

Fig. 15b (cont.)

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

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(54) Data recording/reproducing apparatus using a recording disk.

(57) An equalizer apparatus is to be applied to a disk recording medium of DBF, for which there is used a sampling clock reproduced from the clock pit recorded on a disk recording medium. A fixed equalizer block comprising an analog to digital converter, a memory and a two-dimension equalizer suppresses the wave interference from the adjacent tracks and can reduce the error rate of the reproduced data by cross-talk even in case of narrowing of the track pitch. Further, by adding to the equalizer a sign detector, an FIR low-pass filter and a coefficient control circuit to make it a blind equalizer block, the interference fluctuation attributed to linear recording density, recording power irregularity, light spot, tracking error, etc. can be automatically compensated to suppress such fluctuation. Further, By the construction of the blind equalizer block, the errors of clock timing and its fluctuation can be automatically compensated with good efficiency.

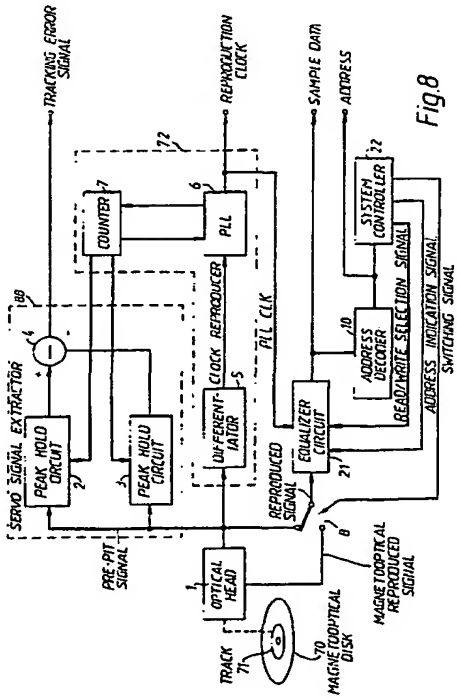

Fig.8

EP 0 375 342 A3

BNSDOCID: <EP_____0375342A3_I_>

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 31 3251

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 219 037 (SHARP K.K.) * Page 7, line 6 - page 10, line 4; figure 3 *	1-2	G 11 B 7/00 G 11 B 20/10
A	EP-A-0 288 114 (PHILIPS AND DUPONT OPTICAL CO.) * Column 9, lines 14-52; figure 7 *	1-2	
A	US-A-4 564 869 (H. BAUMEISTER) * The whole document *	1-2,3,5,7	
A	US-A-4 064 397 (H. SAKAKI et al.) * The whole document *	1-2	
A	EP-A-0 029 550 (OLYMPUS OPTICAL CO., LTD) * Page 13, line 10 - page 14, line 10; figure 18 *	3,5,7	
A	EP-A-0 138 274 (N.V. PHILIPS' GLOEILAMPENFABRIEKEN)	3,5,7	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	PATENT ABSTRACTS OF JAPAN, vol. 5, no. 182 (P-90)[854], 20th November 1981; & JP-A-56 111 116 (SANYO DENKI K.K.) 02-09-1981	3,5,7	G 11 B H 04 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	02-05-1991	KELPERIS K.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
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BNSDOCID: <EP_____0375342A3_I_>

European Patent Office

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid.

namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

X LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions.
namely:

1. Claims 1-2: Data recording and reproducing apparatus.
2. Claims 3-9: Equalizer apparatus.

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid.

namely claims:

☐ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.

namely claims: